UPGRADE OF ABORT TRIGGER SYSTEM FOR SUPERKEKB

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Abstract

The beam abort system was installed in KEKB to protect the accelerator equipment and the Belle detector, and for radiation safety, from high current beams. For SuperKEKB, the new abort trigger system has been developed. It collects more than 130 beam abort request signals and issues the beam abort trigger signal to the abort kickers. The request signals are partially aggregated in local control rooms located along the SuperKEKB ring and finally aggregated in central control room. In order to increase the system reliability, the VME-based module and the E/O module was developed, and all the abort signals between the modules are transmitted as optical signals. The system also has the timestamp function to keep track abort signal received time. The timestamps are expected to contribute to identify the cause of the beam abort. Based on the feasibility tests with a prototype module, the new module design has been improved and fixed. This paper describes the details of the new abort trigger system.

INTRODUCTION

SuperKEKB is the upgrade of the KEKB asymmetric energy electron-positron collider in Japan [1]. The designed luminosity is 40 times as high as the peak luminosity of KEKB.

SuperKEKB consist of two storage rings, low-energy ring (LER) and high-energy ring (HER). Each ring has a beam abort system to protect the accelerator equipment and the Belle detector, and for radiation safety, from high current beams. The abort trigger system collects more than 130 beam request signals and issues a beam abort trigger signal to abort kickers.

In KEKB, the modules of the abort trigger system were connected with twisted pair cable to transmit the electrical request signals and low pass filters were inserted to reduce electrical noise. The low pass filters caused time delay and the total system response time was about 100 μs. For SuperKEKB, the optical request signals are transmitted and the low pass filters have been removed. The response time is improved to be less than 20 μs.

The new system has the timestamp function to keep track of the abort signal received time. The resolution of the timestamp is 0.1 μs. It is expected to contribute to identify the cause of beam abort.

This paper describes the design and the status of the new abort trigger system.

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SYSTEM DESIGN

Modules

The system is composed of two kinds of modules. First is 2ch E/O module which converts electrical signals from abort request source to optical signals. It can receive 3 kinds of electrical inputs: TTL, RS422, or relay, and can treat the input as active-high or active-low. They are set by slide switches in front panel. Figure 1 shows picture of the 2ch E/O module.

Figure 1: Picture of the 2ch E/O module. Input type and polarity can be set by slide switches (1424).

Second is VME-based 8ch beam abort optical input module (18K15). It gathers 8 optical signals and output an OR optical signal. Since it latches the input signals until reset, pulse input can also be detected and it keeps outputting once request signal is detected. Above functions are processed on FPGA, software is not running on the module. The module can be controlled and monitored via VMEbus. Figure 2 shows picture of the VME-based 8ch beam abort optical input module.

Figure 2: Picture of the VME-based 8ch beam abort optical input module (18K15).

Timestamps

Abort request signals are usually occurred sequentially. Therefore an order of the request signals are important to identify a cause of the beam abort. The new abort trigger system records timestamps when it received the request signal. The timestamps reveal the order of sequential request signal.

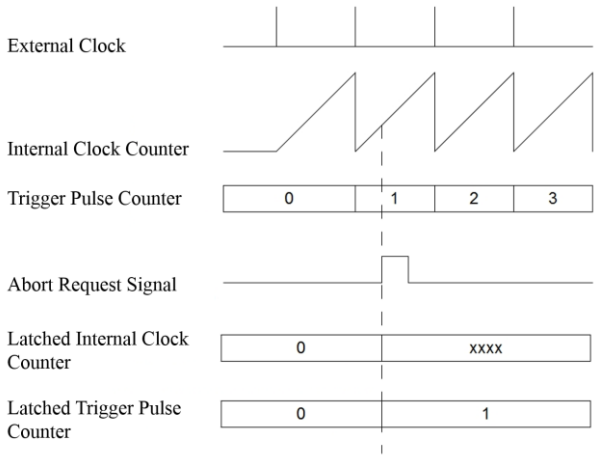

Figure 3: Timing diagram of two counters for timestamps. Internal clock counter counts up at 10 MHz. When the module detects an abort request signal the counters are latched until reset.

The timestamps are generated from two counters, an internal clock counter and a trigger pulse counter, in 18K15. The internal clock counter count up at 10 MHz synchronized to FPGA operation clock. The trigger pulse counter counts an external clock. Each counter is 32-bit and cleared when the module is reset. The internal clock counter is also cleared when the external clock input is detected. After the module reset, each counter starts to count up after the external clock is detected. The external clock synchronize the counters of the all modules in the system. When the module detects an abort request signal the counters are latched until reset. Figure 3 shows the timing diagram of the counter.

The resolution of the timestamp is 0.1 μs since the internal clock counter counts up at 10 MHz. We can notice relative time differences from the counters. However absolute time cannot be calculated without software processing. We can calculate absolute time with the time when an external clock source send a signal.

System Configuration

Figure 4 shows entire system configuration. The electrical abort request signals from equipment are converted to optical signals on 1424 E/O modules. The optical signals are partially aggregated in Local Control Rooms (LCR) located along the SuperKEKB ring and finally aggregated in Central Control Room (CCR). The longest distance from LCR to CCR is 2 km and its transmission time is about 10 μs.

The system needs external clock source to synchronize the timestamp among 18K15s. We use a software trigger system [2] as external clock. It provides the synchronization pulse and/or the interrupt signal to Input/Output Controllers (IOCs) or devices. The time when the software trigger system send a synchronization trigger is recorded on the IOC at CCR.

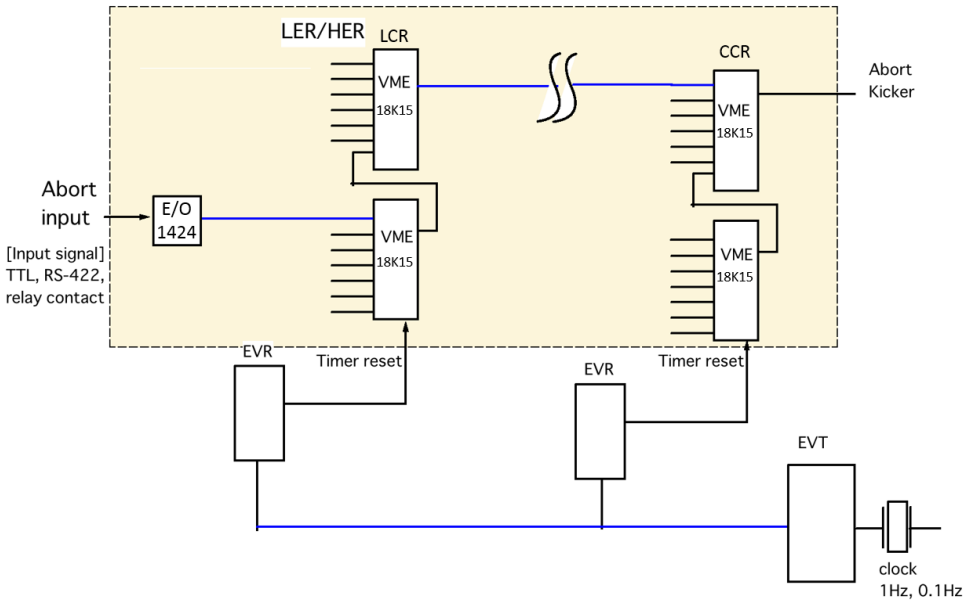

Figure 4: Schematic diagram of the abort trigger system for SuperKEKB. Abort request signals are converted to optical signals on E/O modules and aggregated on VME-based modules. The signals are partially aggregated in LCR and finally aggregated in CCR. The time when EVT (EVent Transmitter module) send a synchronization trigger is recorded on the IOC at CCR.

PERFORMANCE TESTS

Response time

We have tested the response time of 1424 and 18K15. The setup of the test is shown in figure 5. We have measured TTL outputs of the modules equivalent to optical output. Function generator generates pseudo abort request signal which is 500 ns pulse width.

Figure 6 is result of the test. The system detected 500 ns pulsed request signal. It takes about 150 ns for 18K15 to output after E/O module output. This latency is cable delay and processing time of 18K15. Considering that the longest cable delay from LCR to CCR is 10 μs, the latency is sufficiently low and the latency of the abort trigger system mainly depends on the cable delay.

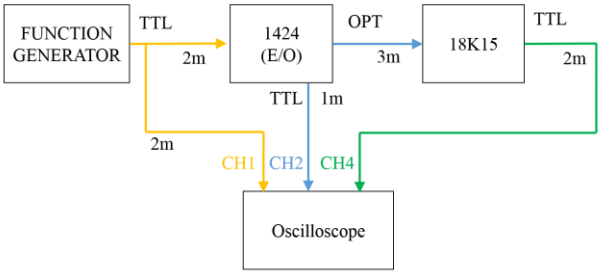

Figure 5: Schematic diagram of the response time measurement.

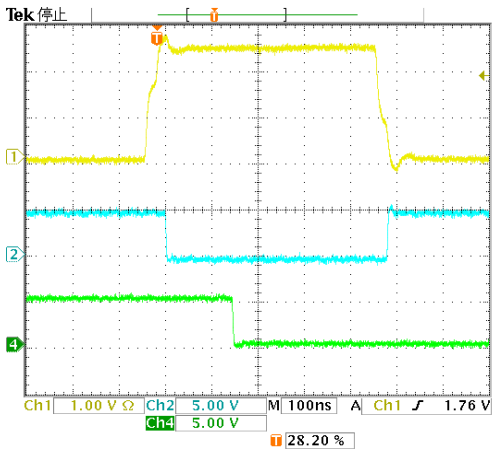

Figure 6: Response of 1424 and 18K15 to 500 ns pulse request signal input. CH1 is pseudo abort request signal generated from Function Generator. CH2 is TTL output equivalent to output of E/O module. CH4 is gathered output on 18K15.

Module control and timestamp

Since the SuperKEKB control system was based on EPICS [3], we have developed EPICS software to control and monitor 18K15.

We have tested the timestamp function with EPICS control system. Abort request signals were input to 18K15 on arbitrary timing and we confirmed latched counters shown in figure 7. The counters revealed an order of abort request signals.

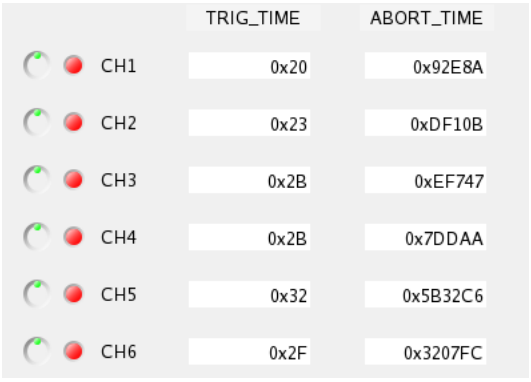

Figure 7: Latched counters of 18K15. TRIG_TIME is the trigger pulse counter and ABORT_TIME is the internal clock counter. The counters show CH1 is the first detected signal.

Figure 8 shows timestamps of time and date format. The timestamps are calculated by software processing based on recorded time which the software trigger system send a synchronization trigger. A relative error among timestamps is several microsecond caused of an error of internal 10 MHz clock on 18K15s and a synchronization error among 18K15s. On the other hand, an absolute error of timestamps is several millisecond caused of an error of the recorded time on IOC at CCR.

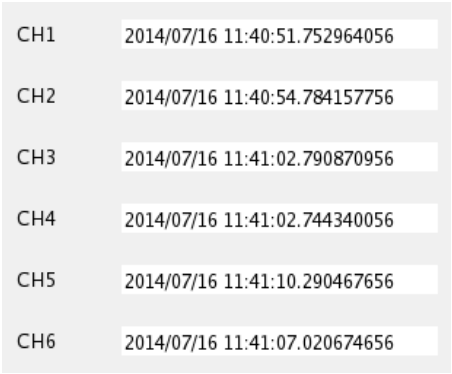

Figure 8: Timestamps of time and date format calculated by software processing.

CONCLUSION

We have developed the new abort trigger system for SuperKEKB. The total response time of the system significantly depends on cable delay and it is improved to be less than 20 μs. The system can record timestamps when it receives abort request signals. Timestamps reveal the order of sequential request signals.

REFERENCES

[1] Y. Ohnishi et al., “Accelerator design at SuperKEKB”, Prog. Theor. Exp. Phys., 2013, 03A011.JACoW.org

[2] T. Naito et al., "Performance of the timing system for KEKB", ICALEPCS’99, Italy, Oct. 4-8, 1999

[3] http://www.aps.anl.gov/epics