DEVELOPMENT OF IMAGE PROCESSING SYSTEM ON EMBEDDED EPICS FOR BEAM DIAGNOSTICS

J. Odagiri, K. Furukawa, T. Obina, M. Satoh, High Energy Accelerator Research Organization (KEK), 1-1 Oho, Tsukuba, Ibaraki, Japan

Abstract

A new image processing system was developed based on EPICS and the FA-M3 PLC made by Yokogawa Electric Corporation. The hardware of the system comprises an F3RP61 CPU module running Linux and an F3UM02 frame grabber module. The CPU functions as an IOC to analyze the raw image data acquired and transferred by the frame grabber module on the PCI-bus, which connects the two modules. A custom record, graphicsRecord, holds the raw image data and the results of analysis as well as parameters set by the user over the network. GUI panels were created by using EDM in order to display the image and to set relevant control parameters into the fields of the graphicsRecord being stationed on the memory of the F3RP61-based IOC. It was confirmed that the developed system is able to acquire image data, analyze them appropriately, and send them over the network to a host computer to display the results of analysis. The design and results on performance measurement of the system is also reported.

INTRODUCTION

It had been common practice to use a desktop PC with frame grabber boards installed in it for beam profile monitoring. This approach allows us to broaden the range of choice of the frame grabber boards and the PC for the purpose. On the other hand, short lifetime of the products and less reliability of the hardware forces us to replace the system frequently to increase burden in maintaining the system in the long run.

In order to solve the problem, we have adopted embedded technology with Experimental and Industrial Control System (EPICS) running on a Programmable Logic Controller (PLC) made by Yokogawa Electric Corporation [1]. Fig. 1 shows the image processing system under test. The main specifications of the F3UM02 frame grabber module are listed in Table 1.

HARDWARE CONFIGURATION

The system comprises an F3RP61 CPU, which runs Linux as its Operating System (OS), and an F3UM02 frame grabber module. The two modules are connected with each other by using not only the PLC-bus on the backplane but also an additional PCI-bus. Both of the modules have a PCI- connector on the side panel to stack them for faster data transfer. The image data acquired with the frame grabber module is transferred to the F3RP61-based CPU by using DMA. The CPU executes the Input / Output Controller (IOC) core program of EPICS on Linux. The IOC analyzes the raw image data and sends it with analyzed results to a host computer which functions as an Operator Interface (OPI) of EPICS.

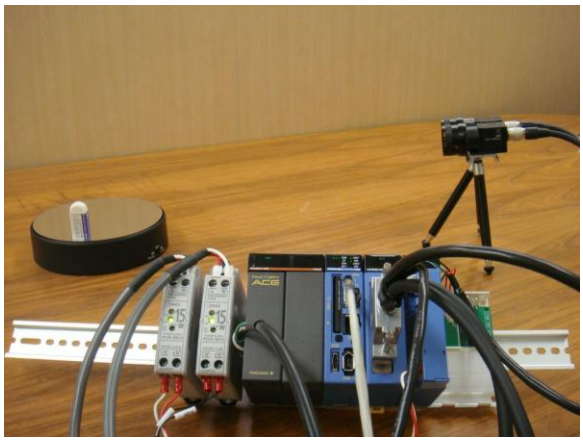

Figure 1: Image processing PLC unit under test. The left most black module (two slots) is the power supply module. The F3RP61 CPU comes to the right of the power supply module. The module just right to the CPU module is the F3UM02 frame grabber module.

Table 1: Main Specifications of F3UM02

Item	Specification
Number of Channels	2ch
Compatible Camera Types	Single Tap (8bits/pixel) Dual Tap (bits/pixel) RGB Colour (24bits/pixel)
Max. Connections	6 monochrome cameras
Resolution of Digitizer/Channel	8 bits
A/D Converter Frequency	100 MHz

SOFTWARE DEVELOPMENT

Record Support

An existing spherical record type, graphicsRecord, which had been created for a seat-gas beam profile monitor was used with some modifications for the analysis of raw image data, such as subtraction of background image, calculation of the projection to both horizontal and vertical directions, searching the peak position in the projection, calculation of the total amount of the light and so forth [2].

Device Support

A new device support module was developed in order to interface graphicsRecord with the hardware. The device support makes the instance of graphicsRecord be processed upon every acquisition of a new image frame by issuing an "I/O_interrupt" scan request. What the device support does is just to transfer the raw image data from the hardware into the buffer of an instance of graphicsRecord. All the other processing of raw image data is subject to the graphicsRecord module.

Operator Interface

Extensible Display Manager (EDM) [3] was chosen for developing the Graphical User Interface (GUI) of the image processing system since it has a type of object which can display an array of data in the form of a two dimensional array of arrays. The feature enables us to display image on the GUI panel from one dimensional array of data stored in the buffer of a graphicsRecord instance as shown in Fig. 2.

TEST OF BASIC FUNCTIONS

To confirm that the device and record support modules function as expected, we have tested the system with a simple object. (See, Fig. 2). The result showed that:

- Captured image was successfully transferred from hardware to the buffer of an snstance of the graphicsRecord.
- Image analysis, such as, creation of projection to both horizontal and vertical directions, peak search, subtraction of background (See, Fig. 3) were successfully executed with the graphicsRecord module.
- The raw image and analyzed results were successfully transferred to the host computer to display them on the EDM-based panel.

All the monitoring and control operations were done via Channel Access (CA) of EPICS which connects F3RP61-based IOC and the host computer over the network.

PERFORMANCE MEASUREMENT

In such a system like PLC, where hardware resource is rather limited, a performance can be an issue. The performance measurement was also done by monitoring CPU power consumption with running the system with various different conditions. The CPU loads measured when no image analysis and no channel access activities were listed in Table 2. Table 3 and Table 4 list the CPU loads measured in case only one of the analysis of raw image or the CA activity between the F3RP61-based IOC and the host computer was in execution. In this measurement, the frame grabber module, F3UM02, was running in external trigger mode and a DC output module was used as the trigger source. While all the tables are subject to a case where one channel of image is being acquired, we have confirmed that the results scale with the number of channels by using two cameras.

More detailed tests revealed that creating projection data costs a lot more than other analysis and making it the most part of the cause of CPU power consumption.

Table 2: CPU Power Consumption
(No Analysis, No Channel Access)

Repetition Period	CPU Load (Typical)	CPU Load (Max.)
1 second	3.00 %	4.00 %
0.5 second	3.70 %	7.30 %
0.2 second	16.0 %	17.0 %
0.1 second	31.0 %	32.6 %

Table 3: CPU Power Consumption
(Only Analysis)

Repetition Period	CPU Load (Typical)	CPU Load (Max.)
1 second	18.6 %	19.0 %
0.5 second	37.0 %	37.3 %
0.2 second	91.3 %	91.9 %
0.1 second	N.A.	N.A.

Table 4: CPU Power Consumption
(Only Channel Access)

Repetition Period	CPU Load (Typical)	CPU Load (Max.)
1 second	6.70 %	7.30 %
0.5 second	13.7 %	14.0 %
0.2 second	34.0 %	35.0 %
0.1 second	69.0 %	70.0 %

SUMMARY

A new image processing system was developed based on an embedded EPICS technology by using a PLC's CPU which executes Linux as its OS and a frame grabber module of the PLC. A special record, graphicsRecord, was ported onto the F3RP61-based IOC and a new device support was developed to interface the record with the hardware. The test results of the system showed that the developed software woks as expected. The result of performance measurement showed that creating projection data is the most part of the cause of CPU power consumption and gives the limit of the repetition rate of image analysis or the number of channels of image data which the developed system can handle.

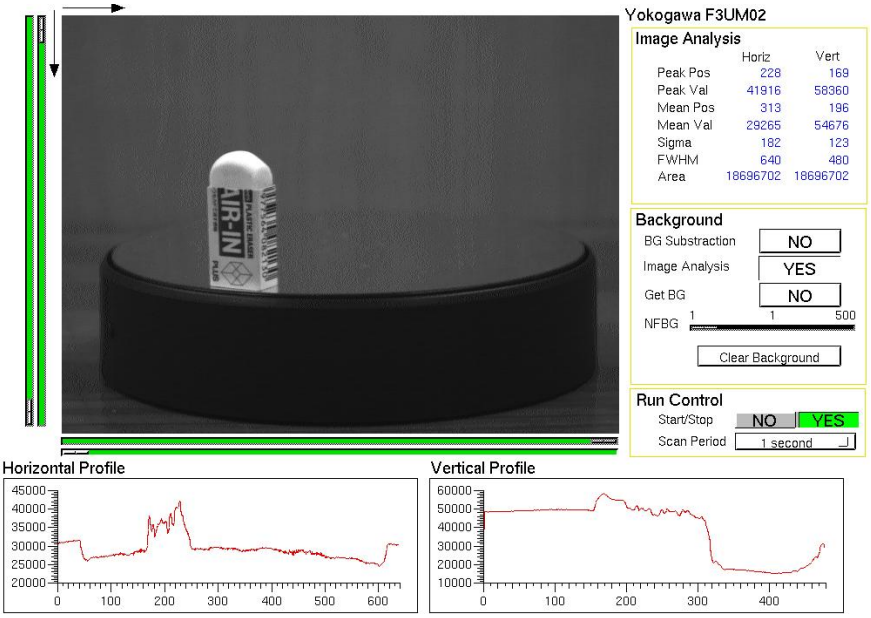

Figure 2: EDM-based graphical user interface. The numbers and buttons at the right side of the image shows the results of analysis and control channels respectively. Horizontal and vertical profiles are shown in the lower part of the GUI.

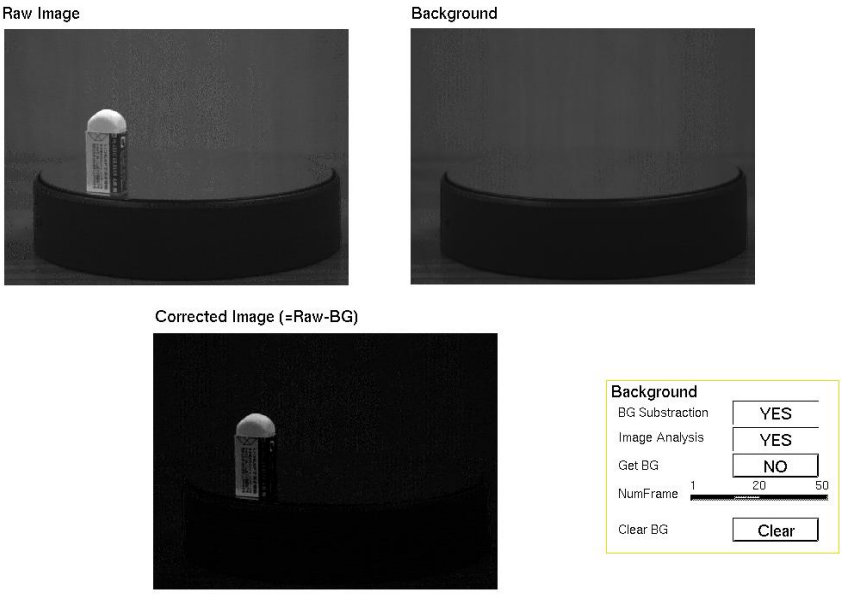

Figure 3: Subtraction of background from raw image. The left side of the upper image shows the raw data. The right side of the upper image shows background data. The result of subtraction is shown in the lower image.

REFERENCES

[1] J. Odagiri et al., "Application of EPICS on F3RP61 to Accelerator Control", Proc. of the 2009 International Conference on Accelerator and Large Experimental Physics Control Systems (ICALEPCS2009), Kobe, Japan, Oct. 12-16, 2009.

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[3] http://www.aps.anl.gov/epics/docs/USPAS2007/lectures/EDM.odp