DIGITAL RF CONTROL SYSTEM FOR 400-MEV PROTON LINAC OF JAERI/KEK JOINT PROJECT

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Abstract

At the proton linac of the JAERI and KEK Joint Project, an accelerating electric field stability of +-1% in amplitude and +-1 degree in phase is required for the RF system. In order to accomplish these requirements, a digital feedback system is adopted for flexibility of the feedback (FB) and feed forward (FF) algorism implimentation. FPGAs are used for the real-time FB system. A DSP board is also utilized for data processing and communication between FPGAs and a crate control CPU (Host).

1 INTRODUCTION

Twenty 324 MHz klystrons are used in the linac of the Joint Project. Each klystron delivers rf power to a one or two-cavity module. As for the digital rf control system, LLRF (low-level rf) control with DSPs is successfully operated for the superconducting cavities in the TTF at DESY[1]. In the case of a normal conducting cavity, a shorter loop delay is necessary for the stability requirements (such as +-1% in amplitude and +-1 degree in phase). In our system, the digital FB system using the FPGAs on a DSP board is adopted in order to minimize the FB loop delay. A DSP board 'Barcelona' (Sepctrum Signal Processing Inc.), having four DSPs (TI-C6701) acts as the data/program exchange between the FPGAs and the HOST. Two FPGAs (Xilinx XCV600E), which work for the main FB control, are installed in the PEM (Processor Expansion Module).

2 LLRF FB HARDWARE

All of the LLRF system components are installed in a compact PCI (cPCI rack). A total of five boards (CPU, DSP, RF & CLK, Mixer & I/Qmod, and control I/O) are used, as shown in Fig.1. The timing, trigger, and control I/O signals are transferred through the user Bus (J5) in the cPCI rack.

The rf and clock generator (RF & CLK) board receives a 12 MHz signal through an optical fiber [2] from a master oscillator. Timing clock (f_{Tim}, 12 MHz; f_{Trig}, 48 MHz), LO (f_{LO}, 312 MHz), RF (f_{RF}, 324 MHz) signals are generated and phase-locked with the 12-MHz external reference signal. The mixer and I/Q modulator board (Mixer & I/Qmod) includes an IQ modulator (AD8345) for delivering the rf signal to the klystron, and an active mixer (AD8343) for downconverting the rf signal from the cavity to the 12-MHz IF signal.

Each FPGA is connected to two 14bit-ADCs (AD6644) and two 14bit-DACs (AD9764). The digital FB is carried out through one of the FPGAs (FPGA1). Another FPGA

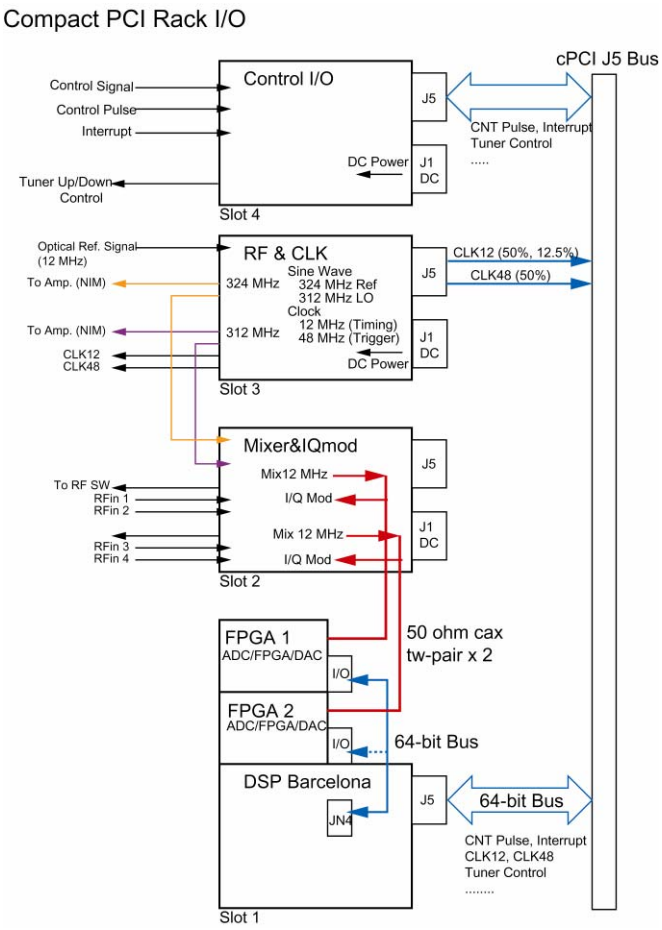

Fig.1 cPCI system

(FPGA2) measures the I/Q components of the klystron output (in front of the cavity coupler) for the cavity tuner control. The total FB loop delay is considered to be less than 1 μs, including all of the rf components, cables, ADC, DAC and FPGA.

3 LLRF SOFTWARE

3.1 Digital FB software (FPGA1)

The simple PI (proportional and integral) control is adopted for the FB so as to minimize the FB delay. The algorism is schematically shown in Fig. 2. The IF signal (12MHz) is converted to a 14 bit digital signal with a 48 MHz sampling rate. The values are defined as I, Q, -I, -Q, step by step with a 90-degree separates. The measured I/Q components are rotated for the loop phase calibration for input signals. In the case of SDTL(separated drift tube linac), where two cavities are driven by a klystron [3], a

vector-sum (or weighted vector sum) is applied. The set tables (FB and FF) are given every 1 μs during the 600-μs rf pulse, and the measured data are stored in the FPGA block memory.

3.2 RF output field measurement (FPGA2)

The I/Q components of the rf output from the klystron are measured at FPGA2. The algorism is the same as that of FPGA1. The measured data are stored in and read out from the DSP through the PEM ports. The data are converted from I/Q components to the amplitude and the phase in the DSP. The phase difference between the cavity and the klystron is compared with those at on-resonance. In the case that the tuning error calculated from the compared phase-difference shift is higher than a specified value, the DSP starts to control the cavity tuner. By communication with the tuner PLC through the control I/O board.

4 FB SIMULATION

A baseband analysis, where only the bandwidth near the operation frequency is considered, enables a simplified state-space equation:

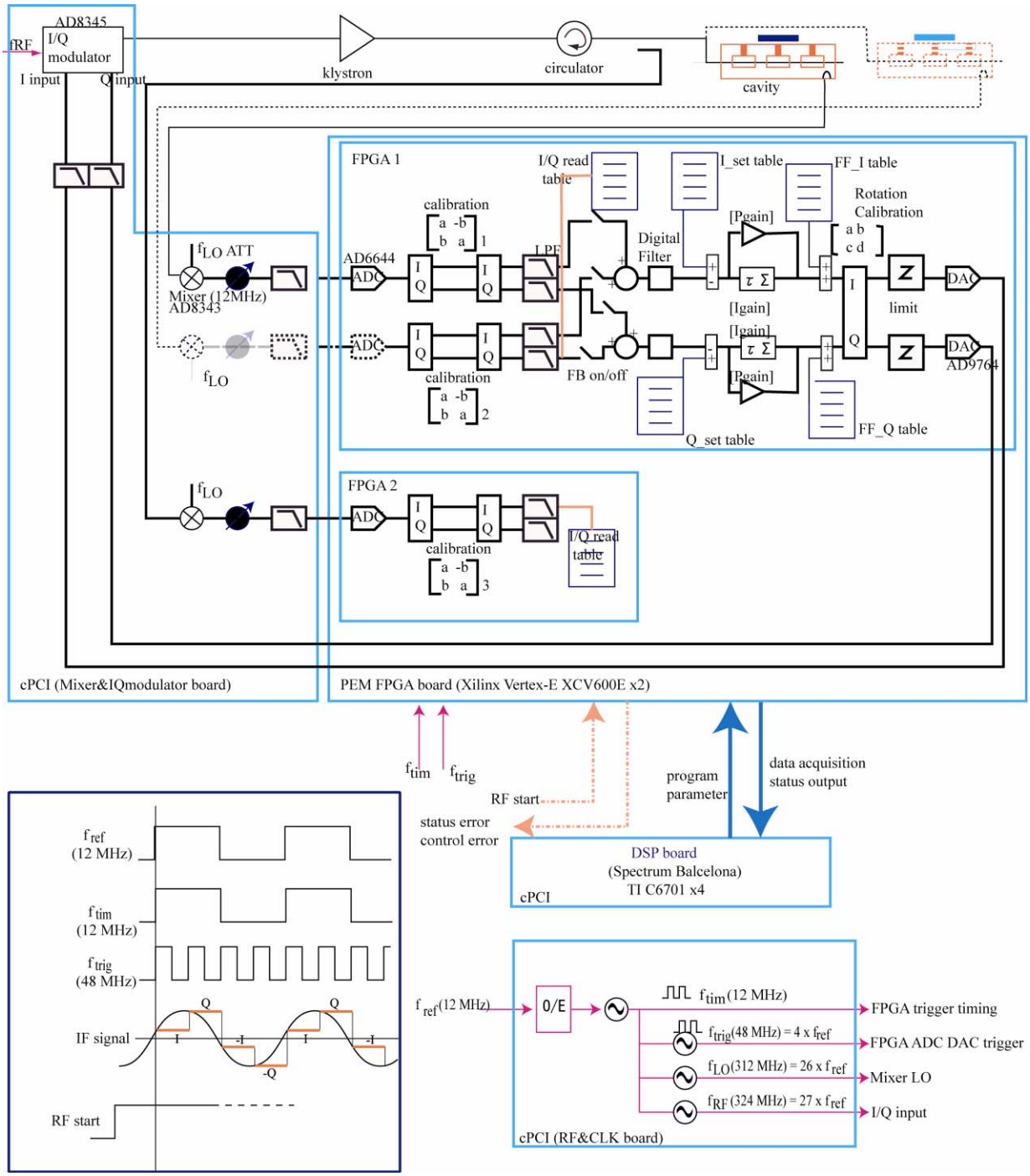

Fig. 2 FB system using FPGAs.

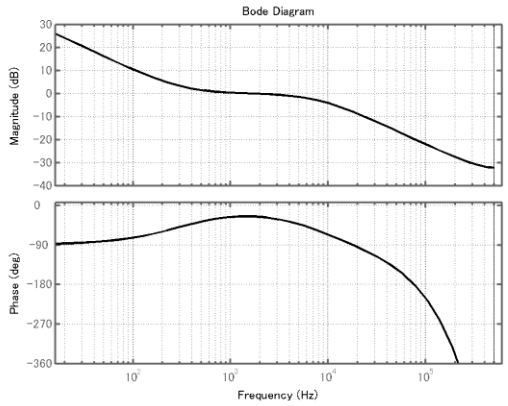

Fig. 3 Bode plot for the digtal system (calculation).

$$\frac{d}{dt}\begin{bmatrix} V_I \\ V_Q \end{bmatrix} = \begin{bmatrix} -\omega_{1/2} & -\Delta\omega \\ \Delta\omega & -\omega_{1/2} \end{bmatrix}\begin{bmatrix} V_I \\ V_Q \end{bmatrix} + \frac{\omega_0}{2}\frac{R}{Q}\begin{bmatrix} I_I \\ I_Q \end{bmatrix},$$

$$\omega_{1/2} = \frac{\omega_0}{Q_l},$$

$$\Delta\omega = \omega_{cavity} - \omega_{rf}.$$

Since the rf amplifier has a wider bandwidth of about 1 MHz [4], the dominant rf device to determine the FB characteristics is the cavity.

The PI control in the system can be described as

$$SYS\_CONT(s) = K_p(1 + \frac{K_i}{s}) .$$

The cavity, FB delay and PI-control play essential roles in the FB system. A bode plot of the open loop system is shown in Fig. 3. A delay time of 1 μs, Q_l of 20,000, K_p=1 and K_i=1e5 are used in the calculation. A gain margin of 9.6 is obtained for the parameter. For practical operation, the half number of the gain margin (K_p=4~5), is considered to be stable [5].

5 MEASUREMENTS

Preliminary experiments with the cavity were carried out. A schematic drawing of the experiments is shown in Fig. 4. The trapezoid field input pattern was examined. The klystron output is connected to a DTL (drift tube linac) high-power test tank having a Q_l value of about 20,000. The results are shown in Fig. 5. The K_p and K_i were 4 and 1e5, respectively. The raw integer data are displayed in the figure. The calibration number should be multiplied in order to obtain the real cavity field. In this

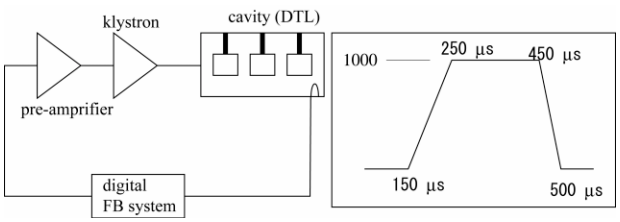

Fig. 4 Schematic of the FB experiment.

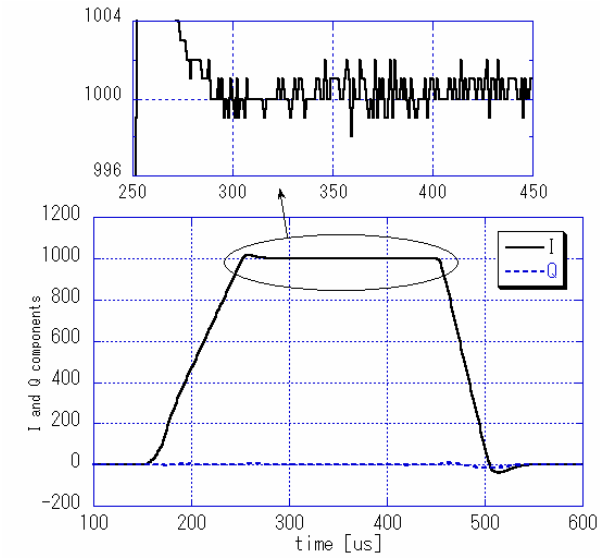

Fig. 5 Measured electric field at the DTL cavity system.

case, a setpoint (1,000) is established after 300 ns of the settle time. The error on the flat top is the quantum error level (about +-2) corresponding to +-0.2%.

6 SUMMARY

The proton linac at the joint project requires an rf stability of +-1% in amplitude and +-1 degree in phase. In order to satisfy these requirements, a fast digital feedback system using FPGAs is adopted. The simulation indicates operating PI constants of K_p=4 and K_i=1e5. Cavity experiments were successfully operated with these simulated parameters. A stability of +-0.2% was obtained at the FB region, which satisfies the specification.

7 REFERENCES

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