Diamond Timing System Modules

EPICS Meeting

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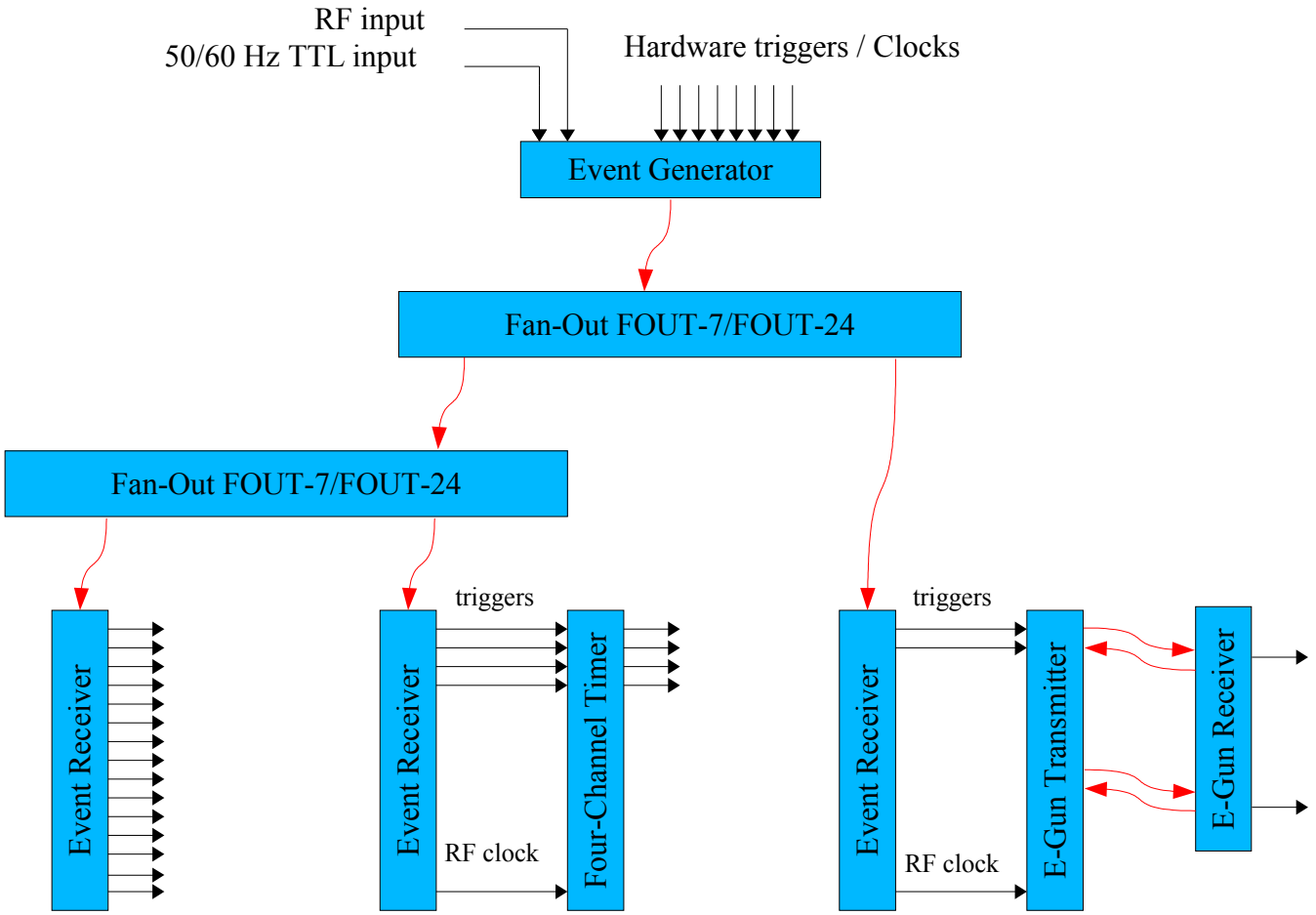
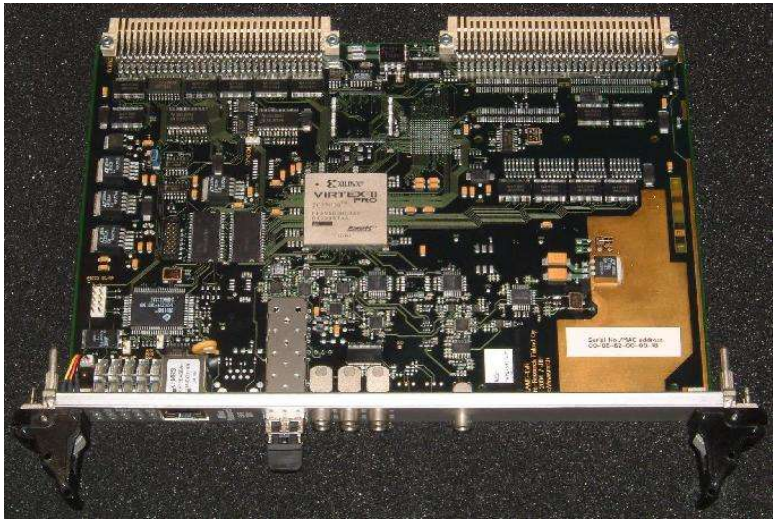
Timing Event System Overview

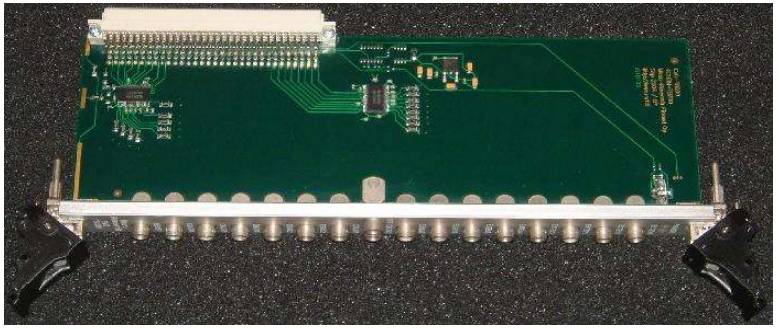


Event Generator EVG-200



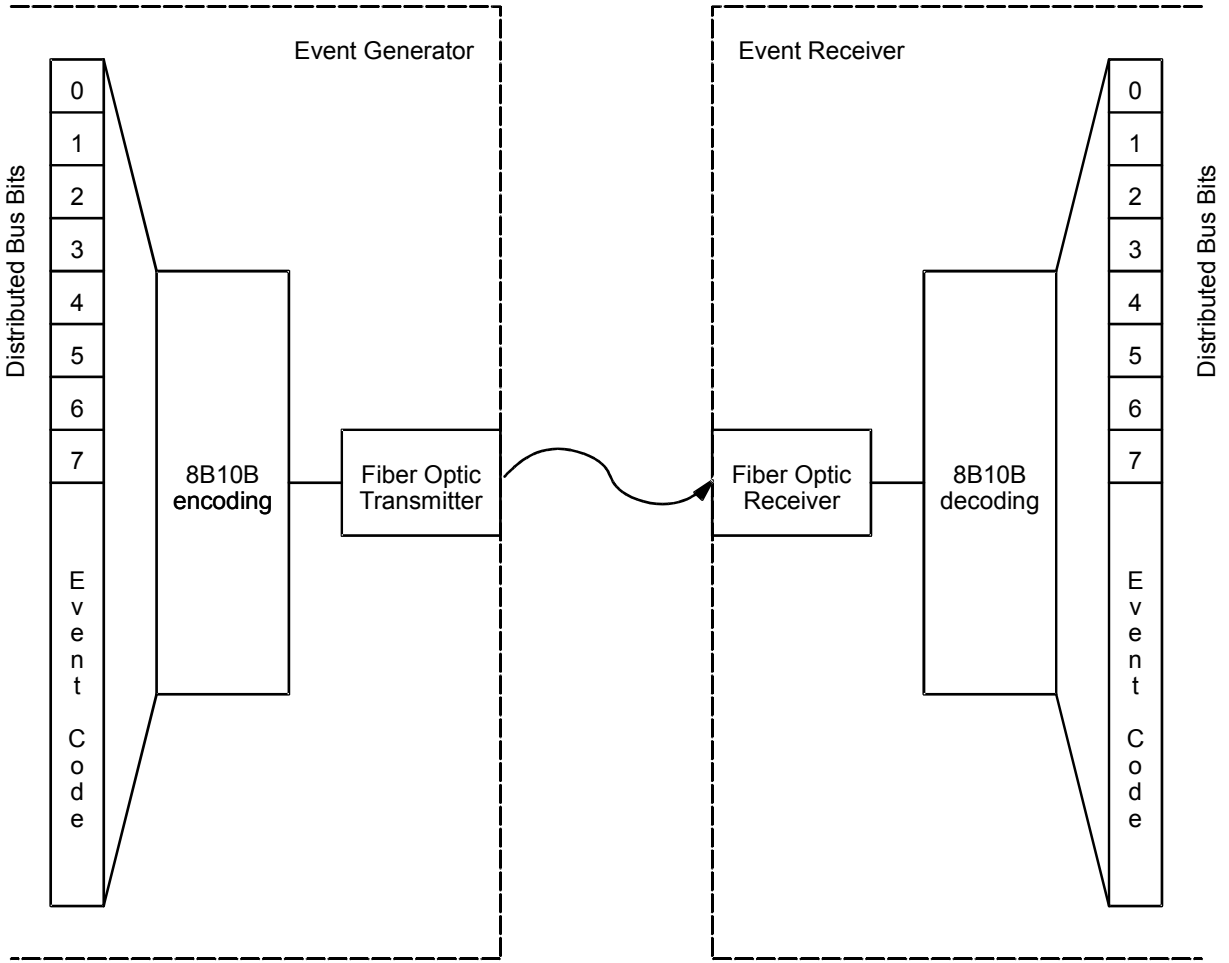
- Event clock rate 50 MHz to 125 MHz
- Transmitted bit rate 1.0 Gbps to 2.5 Gbps
- RF to Event clock dividers /4, /5, /6, /8, /10 and /12
- TTL front panel input for synchronisation e.g. to 50/60 Hz AC line voltage
- 256 Event codes
- 2 Event sequencers
- 8 Distributed bus bits
- 8 Multiplexed counters

Event Generator Transition Board EVG-TB-200

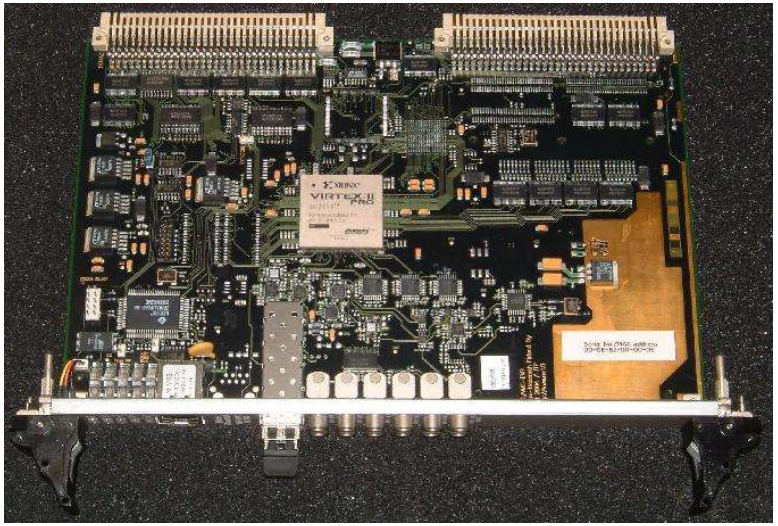


- 8 Trigger event inputs
- 8 Distributed bus inputs
- External reset input

Event System Frame Structure

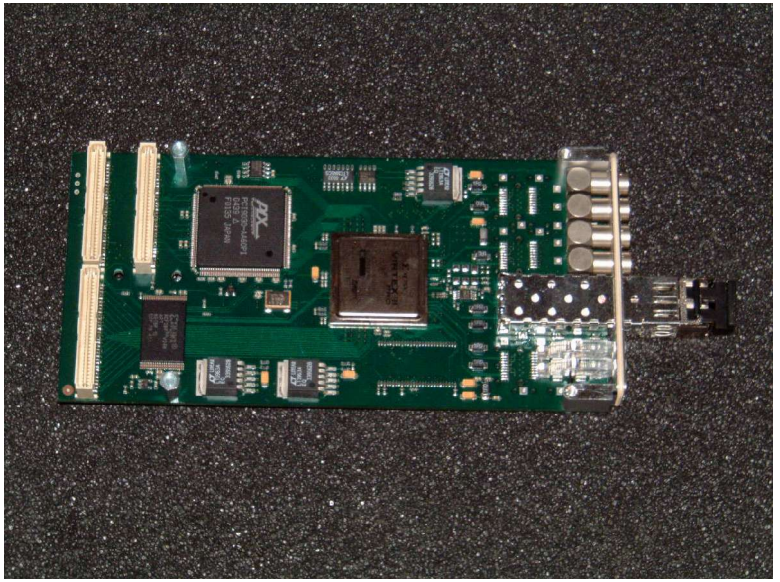


VME Event Receiver VME-EVR-200 and VME-EVR-RF-200



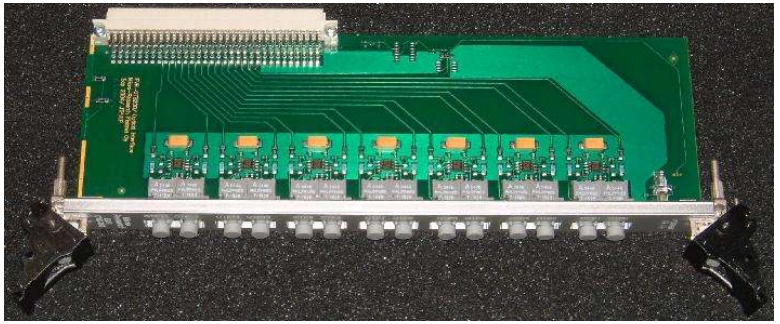
- 32 Hardware outputs through P2:
  - 4 PDP outputs: 32 bit counters for pulse width and delay, 16 bit prescaler
  - 7 TEV Trigger event outputs
  - 14 OTP/8 DBUS outputs: 32 bit counter for pulse delay, 16 bit counter for pulse width
  - 7 OTL Level outputs
- RF clock recovery (VME-EVR-RF-200)
  - 20 bit pattern repeated with event clock rate
- 7 programmable front panel outputs: 5 TTL, 2 differential LVPECL
- Timestamping with 32 bit seconds counter and 32 bit fast counter (up to event clock rate)
- Event FIFO for storing events with timestamp
- Front panel external event trigger input

PMC Event Receiver PMC-EVR-200



- 32 Hardware outputs through Pn4:
  - 4 PDP outputs: 32 bit counters for pulse width and delay, 16 bit prescaler
  - 7 TEV Trigger event outputs
  - 14 OTP/8 DBUS outputs: 32 bit counter for pulse delay, 16 bit counter for pulse width
  - 7 Level outputs
- 3 programmable TTL front panel outputs
- Timestamping with 32 bit seconds counter and 32 bit fast counter (up to event clock rate)
- Event FIFO for storing events with timestamp
- Front panel external event trigger input

Event Receiver Transition Boards

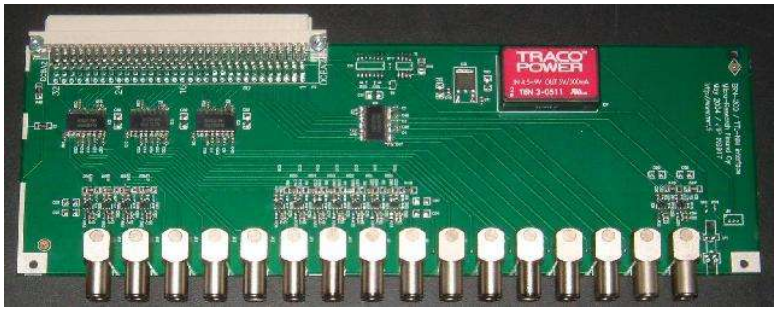


Optical Transition Board EVR-OTB

- 14 Agilent HFBR-1528 Versatile Link Transmitters
- All OTP outputs

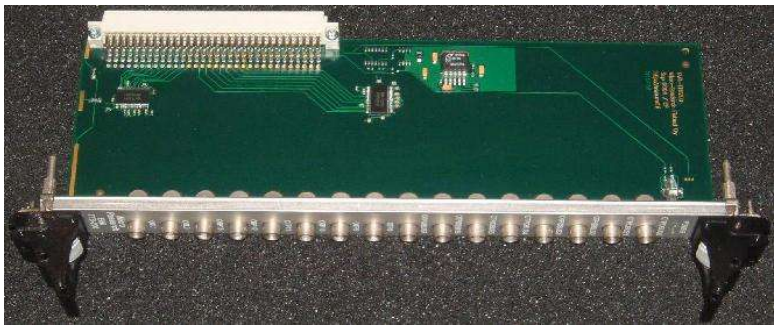
High Speed Optical Transition Board EVR-HTB

- 4 Agilent HFBR-1528 Versatile Link Transmitters
- 10 Agilent HFBR-1414 Transmitters
- All OTP outputs



TTL/NIM Transition Board EVR-NTB

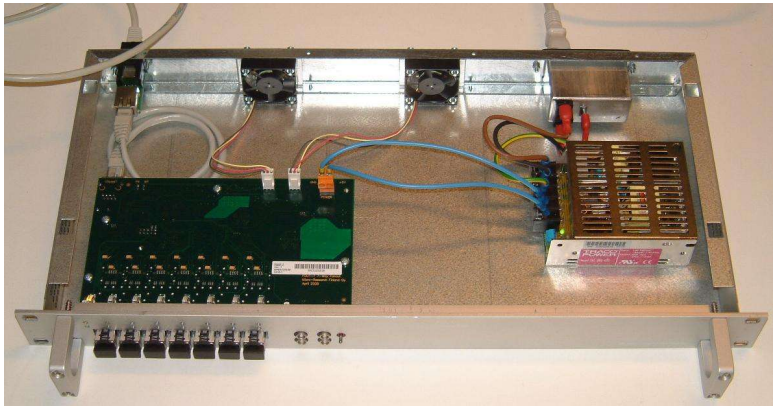
- 16 Stacked Lemo connectors
- 13 NIM-level outputs (2 PDP, 7 OTP, 4 OTL)
- 19 TTL-level outputs (2 PDP, 7 TEV, 7 OTP 3, OTL)



TTL Transition Board EVR-TTB

- 16 Single Lemo connectors
- 16 TTL-level outputs (14 OTP, 2 OTL)

7-Way Fan-Out FOUT-7

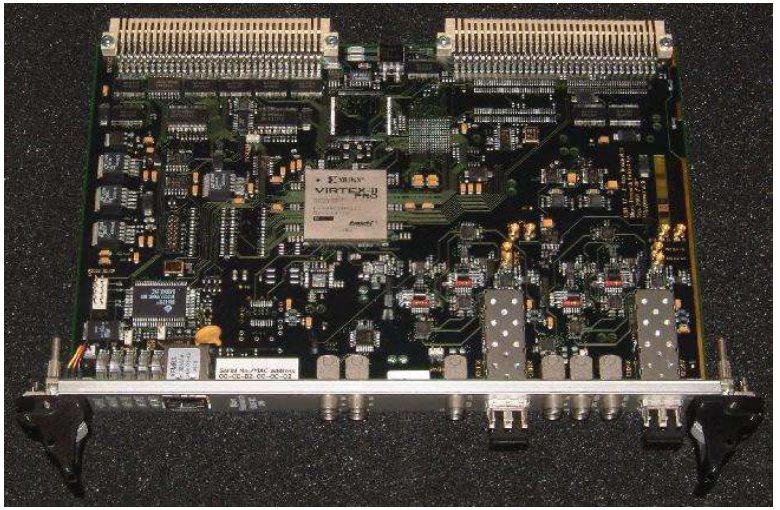


- Distribute optical event stream, optionally RF signal
- 19” rack mount box
- 7 SFP transceivers
- 2 differential LVPECL outputs (stacked Lemo)
- Configurable for 7-way or 6+1-way operation
- 10BaseT network interface for monitoring temperatures, fan speeds, etc.

24-Way Fan-Out FOUT-24

- Distribute optical event stream
- 19” rack mount box
- 24 SFP transceivers
- 10BaseT network interface for monitoring temperatures, fan speeds, etc.

E-Gun Driver Set GUN-TX-200 and GUN-RC-201



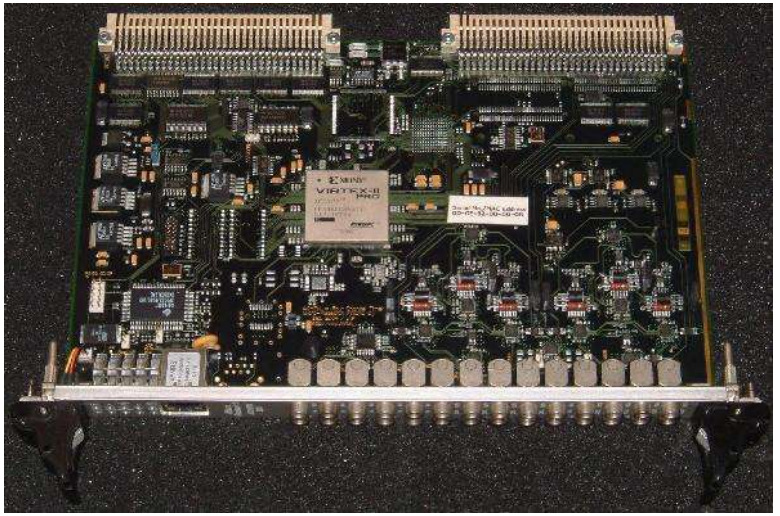
E-Gun Transmitter

- Transfers two trigger pulses to E-Gun at high voltage
- Utilises multimode fibre and standard transceivers
- Differential or single-ended RF input (500 Mhz)
- Two differential LVPECL trigger inputs
- Trigger delay adjustable in RF clock steps (0 – 2^{32}-1)
- Delay fine-tuning in ~10 ps steps
- Pulse width adjustable in RF clock steps (4 – 2^{32}-1)
- Feedback signal from GUN-RC available at GUN-TX front panel

E-Gun Receiver

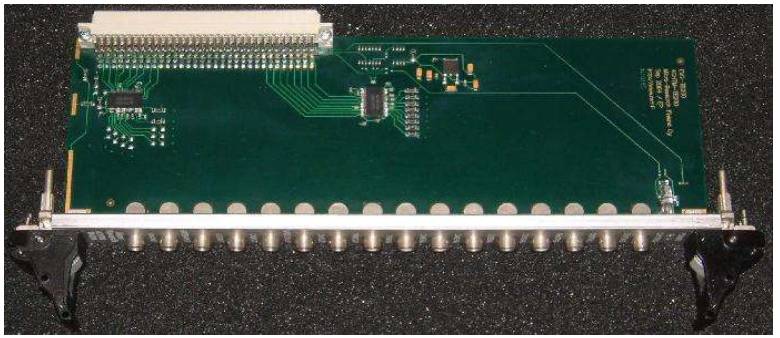
- 10 HP, 3 U HF enclosure
- 24 VDC supply voltage
- 2 BNC outputs 0 – 5 V pulses

Four-Channel Timer 4CHTIM and 4CHTIM-TB



Four Channel Timer

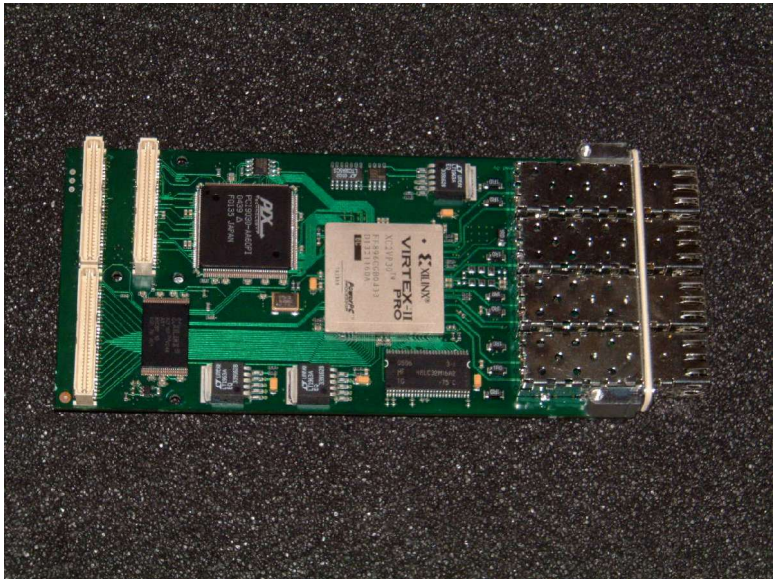
- Four independent delay channels
- Delay programmable in RF clock steps ($0 – 2^{32}-1$)
- Delay fine-tuning in ~10 ps steps
- Width programmable in RF clock steps ($0 – 2^{32}-1$)
- Gated pulses by combining CH1 & CH2 or CH3 & CH4
- Front panel differential LVPECL connections



Four Channel Timer Transition Board

- TTL level signals
- 4 trigger inputs, 1 common trigger input and output
- Enable signals for each channel
- TTL outputs for each channel and gated channels

PMC Prototype Module with Four SFPs



- Xilinx Virtex-II-Pro XC2VP30-6FF896C
- 64 Mbytes SDRAM memory
- Four SFP transceivers
- Programmable clock reference for RocketIO™
- PLX Technologies PCI9030 I/O accelerator
- XCF16P configuration memory

Event System Future Development

Data Transmission

- Programmable size (up to 2 kbytes) buffer transmitted from EVG to EVRs
- Shares distributed bus bandwidth
- May be enabled on demand
- 16 bit hardware checksum
- Software controlled

EVG Cycle Sequencer

- Up to 16384 cycles of 2048 events
- Events stored with 32 bit timestamp

Changes to EVG Hardware

- Direct event clock input option

Future Research / Point of Interest

Running Linux or RTEMS and EPICS on PowerPC with EVR FPGA

- Stand-alone version with network interface?

Allowing transitions in RF frequency

- Frequency range currently limited to 100 ppm

Next Generation FPGA Virtex-IV

- Can the Virtex-IV RocketIO™ be used for timing?
- Event clock rates up to 500 MHz
- Bit rate up to 11 Gbps

Two Way Signaling

- Provide event/data transfer patch from EVRs to EVG