2249A, 2249SG and 2249W

12-CHANNEL ADC

April, 1984

WARRANTY

LeCROY CORPORATION warrants each instrument it manufactures to be free from defects in material and workmanship under normal use and service for the period of 1 year from the date of purchase. Custom monolithics and hybrids sold separately and all spare or replacement parts and repairs are warranted for 90 days. This warranty extends only to the original purchaser and shall not apply to fuses, disposable batteries, or any product or parts which have been subject to misuse, neglect, accident or abnormal conditions of operations.

In the event of failure of a product covered by this warranty, LeCroy will repair and calibrate an instrument returned to the factory or an authorized service facility within one year of the original purchase; provided the warrantor's examination discloses to its satisfaction that the product was defective. The warrantor may, at its option, replace the product in lieu of repair. With regard to any instrument returned within one year of the original purchase, said repairs or replacement will be made without charge. If the failure has been caused by misuse, neglect, accident, or abnormal conditions or operations, repairs will be billed at a nominal cost. In such cases, an estimate will be submitted before work is started, if requested.

The foregoing warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy Corporation shall not be liable for any special, incidental, or consequential damages, whether in contract, tort or otherwise.

IF ANY FAILURE OCCURS, notify LeCroy Corporation or the nearest service facility, giving full details of the difficulty, and include the Model number, serial number, and FAN (Final Assembly Number) or ECO (Engineering Change Order) number. On receipt of this information, service data or shipping instructions, forward the instrument, transportation prepaid. A Return Authorization Number will be given as part of shipping instructions. Marking this RA number on the outside of the package will insure that it goes directly to the proper department within LeCroy. Repairs will be made at the service facility and the instrument returned transportation prepaid.

ALL SHIPMENTS OF LECROY INSTRUMENTS FOR REPAIR OR ADJUSTMENT should be made via Air Freight or "Best Way" prepaid. The instrument should be shipped in the original packing carton; or if it is not available, use any suitable container that is rigid and of adequate size. If a substitute container is used, the instrument should be wrapped in paper and surrounded with at least four inches of excelsior or similar shock-absorbing material.

IN THE EVENT OF DAMAGE IN SHIPMENT to original purchaser the instrument should be thoroughly inspected immediately upon original delivery to purchaser. All material in the container should be checked against the enclosed Packing List. The manufacturer will not be responsible for shortages against the packing sheet unless notified promptly. If the instrument is damaged in any way, a claim should be filed with the carrier immediately. (To obtain a quotation to repair shipment damage, contact the LeCroy factory or the nearest service facility).

DOCUMENTATION DISCREPANCIES OR OMISSIONS. LeCroy Corporation is committed to providing unique, reliable, state-of-the-art instrumentation in the field of high speed data acquisition and processing. Because of the commitment, the Engineering Department at LeCroy is continually refining and improving the performance of products. While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purpose of pulse shape, timing, offset, etc., and, only rarely including minor logic changes. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

ANY APPLICATION OR USE QUESTIONS, which will enhance your use of this instrument will be happily answered by a member of our Engineering Services Department, telephone 914-578-6058 or your local distributor. You may address any correspondence to:

LeCroy Corporation, 700 S Main St.,
Spring Valley, New York 10977, ATTN: Customer Service Dept. or
LeCroy Corporation, 14800 Central S.E.,
Albuquerque, New Mexico 87123
LeCroy Corporation, 1816 Holmes Street, Bldg. E
Livermore, California 94550

European Customers can contact:

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Werderstrasse 48
Postfach 10 37 67
6900 Heidelberg
West Germany

A T T E N T I O N

GATE INPUTS OF THE 2249SG MUST BE DOUBLE NIM AMPLITUDE (-1.4 VOLTS). SEE SECTION 2.3.

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF UNIT TO AVOID POSSIBLE DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LISTS, AND ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

A T T E N T I O N

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TECHNICAL DATA

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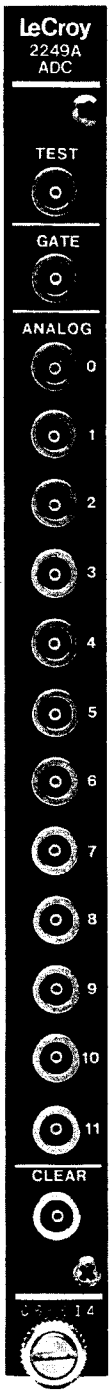


CAMAC Model 2249A
12 Channel A-to-D Converter

FEATURES:

* **COMPACT PACKAGING**
  12 channels per single-width module means fewer crates, smaller systems, less gate fan-out.
* **WELL-CONTROLLED PEDESTAL**
  Advanced hybrid circuit front end eliminates peak shifts and/or constant calibration.
* **EXCELLENT INPUT IMPEDANCE MATCH**
  Minimizes possibility of digitizing input reflections.
* **10-BIT RESOLUTION**
  One part in 1024.
* **WIDEST DYNAMIC RANGE**
  4 times the range of 8-bit ADC's allows broader spectra, better accuracy, simplified setup, prevents small gain shifts from exceeding range of ADC.
* **HIGH SENSITIVITY**
  0.25 picocoulomb per count.
* **NO FEEDTHROUGH**
  Up to 1,000-fold overloads are rejected by fast gate, eliminating spurious data due to out-of-time chamber firings, noise, etc.
* **UNIFORM SENSITIVITY THROUGHOUT GATE INTERVAL**
  No modulation of measurement with position of signal within gate.
* **NO INTERCHANNEL CROSSTALK**
  regardless of input amplitude.
* **WELL-VENTILATED MODULE**
  Low component count, less than one-fifth of competing designs, permits free circulation of air for cooler, more reliable, and longer-lasting operation.
* **FAST CLEAR INPUT**
  enables fast rejection of unwanted data.
* **FULL TEST CAPABILITY**
  F(25) simultaneously injects charge into all ADC's proportional to DC level on front panel (or patch pins on Dataway).
* **FULL LAM FUNCTIONS.**
* **HIGH DIGITIZING SPEED**
  without sacrifice in differential linearity.
* **LAM AND Q SUPPRESSION**
  eliminates readout of empty modules.

The LRS Model 2249A 12-Channel Analog-to-Digital Converter embodies all the operational characteristics which have proved important for general-purpose use in high energy particle physics, including expanded resolution (0.1%), higher sensitivity, excellent stability, faster digitizing rate, LAM and Q suppression, provision for fast clear, calibrating test mode, and flexible LAM options.

These ADCs are specifically intended for use in demanding applications such as particle identification using dE/dx counters, recording x-ray, neutron, or recoil proton energies using lead glass or other total energy absorbtion counters, improving time resolution by correcting for slewing due to variances in counter output amplitudes, monitoring gas threshold Cerenkov counters, and debugging or monitoring proportional or drift chambers.

The Model 2249A contains twelve complete ADC's in a single-width CAMAC module. Each ADC offers a resolution of ten bits to provide 0.1% resolution over a wide 1024-channel dynamic range. The factor of 4 wider range allows operations with broad signal spectra such as are encountered in experiments anticipating fractionally charged particles or covering extensive energy ranges. It also greatly reduces the necessity for careful adjustment of signal strengths to match the limited range of an 8-bit, 256-channel instrument. The input sensitivity of the Model 2249A is 0.25 pC/count for a full-scale range of 256 pc. This is compatible with most available signal sources and no additional buffering or reshaping of any kind is required to digitize nanosecond pulses.

The excellent long-term stability, temperature characteristics, and isolation between ADC channels assure accurate and reliable performance under the demanding conditions encountered in actual experiments. Confirmation of operation and calibration is provided by the unique test feature which allows all twelve ADC's or an entire system to simultaneously digitize a charge proportional to a dc level provided to a front-panel Lemo connector or patched into P_1, P_2 or P_5 of the Dataway connector.

The Model 2249A offers excellent event rate capability through the incorporation of a fast clear and a fast digitizing rate. The fast clear input enables the ADC to begin digitizing on the command of a prompt gate and be reset, if necessary, before the end of conversion on the basis of delayed logic or chamber information. This feature eliminates the long input delay cables now required in these situations.

End of conversion of modules which contain data is flagged by generation of a CAMAC LAM. Readout of modules which do not contain information can be eliminated either by use of the LAM signals or through Q suppression.

August 1982

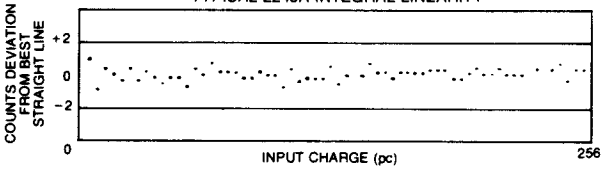
Innovators in Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION • 700 SOUTH MAIN STREET • SPRING VALLEY, N.Y. 10977
TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

SPECIFICATIONS
Model 2249A
12 CHANNEL ADC

Analog Inputs:	Twelve; Lemo-type connectors; charge-sensitive (current-integrating); direct-coupled, quiescently at approximately +4 mV; 50 Ω impedance; linear range normally −2 mV to −1 V; protected to ± 50 volts against 1 μsec transients.
Full-Scale Range:	256 pC ± 5%.
Full-Scale Uniformity:	± 5%.
Integral Non-linearity:	± .25% of reading ± 0.5 pC (12 pC to 256 pC) for >500 Ω source.
ADC Resolution:	10 bits actual, (0.1%).
Long-Term Stability:	Better than 0.25% of reading ± 0.5 pC/week (at constant temperature).
Temperature Coefficient:	Typical, 0; max., ± [.03% of reading (in pC) + .002t] pC/°C (where t = gate duration in nanoseconds, with 50Ω reverse termination).
ADC Isolation:	A 5-volt, 20 ns overload pulse in any one ADC disturbs data in any other ADC by no more than 0.25 pC.
Gate Input:	One gate common to all ADC's; LEMO-type connectors; 50 Ω impedance; −600 mV or greater enables; minimum duration, 10 ns; maximum recommended duration, 200 ns (actual limit approximately 2 microseconds with reduced accuracy; partial analog input must occur within 0.5 μsec after opening gate to preserve accuracy), effective opening and closing times: 2 ns; internal delay, 2 ns.
Fast Clear:	One front-panel input common to all ADC's; LEMO-type connector; 50 Ω impedance; −600 mV or greater clears, minimum duration, 50 ns. (Caution: narrower pulses cause partial clearing.) Requires additional 2.0 μs settling time after clear.
Residual Pedestal:	Typically 1 + 0.03t picocoulombs (where t = gate duration in nanoseconds) with 50 Ω reverse termination.
Test Function:	With CAMAC I present, the positive DC level applied to front panel "Test" input (internal high impedance connection to +12 volts) or optional rear connector P1, P2, or P5 patch points will inject charge with a proportionality constant of −12.5 pC/volt into all inputs at F(25) • S2 time. (With CAMAC I not present, F(25) • S2 will generate the ≈80 ns gate only, providing a measure of residual pedestal only.)
Digitizing Time:	60 μs. By factory option, 8-bit operation at 12.5 μs digitizing time may be provided.
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.
Readout Control:	Ready for readout when LAM signal appears. Refer to ESONE Committee Report EUR4100e and EUR4600e for additional timing details, voltages, logic levels, impedances, and other standards.
Data:	The proper CAMAC function and address command normally gates the 10 binary bits plus overflow bit of the selected channel onto the R1 to R11 (2^0 to 2^{10}) Dataway bus lines.
CAMAC Commands:	Z or C: ADC's and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. Z also disables LAM. I: Gate input is inhibited during CAMAC "Inhibit" command. (Test Function is enabled.) Q: A Q=1 response is generated in recognition of an F(0) or F(2) Read function or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q=0) under any other condition. The Q response for empty modules can be suppressed. (See Q and LAM suppression.) X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated. L: A Look-At-Me signal is generated from end of conversion until a module Clear or Clear LAM. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by Test LAM. Standard option causes LAM to be suppressed for empty modules.
CAMAC Function Codes:	F(0): Read registers; requires N and A, A(0) through A(11) are used for channel addresses. F(2): Read registers and Clear module and LAM; requires N and A; (Clears on A(11) only.) F(8): Test Look-At-Me; requires N and any A from A(0) to A(11) independent of Disable Look-At-Me. Q response is generated if LAM is set. F(9): Clear module and LAM; requires N, S2, and any A from A(0) to A(11). F(10): Clear Look-At-Me; requires N, S2, and any A from A(0) to A(11). F(24): Disable Look-At-Me; requires N, S2, and any A from A(0) to A(11). F(25): Test module; requires N, S2, and any A from A(0) to A(11). F(26): Enable Look-At-Me; requires N, S2, and any A from A(0) to A(11). Remains enabled until Z or F(24) applied. Caution: The state of the LAM mask will be arbitrary after power turn-on.
Q and LAM Suppression:	Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 100) before data is considered useful. A module in which all channels contain less than set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option.
Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e). RF shielded CAMAC #1 module.
Current Requirements:	+24 V at 35 mA; −24 V at 15 mA; +6 V at 850 mA; −6 V at 200 mA.

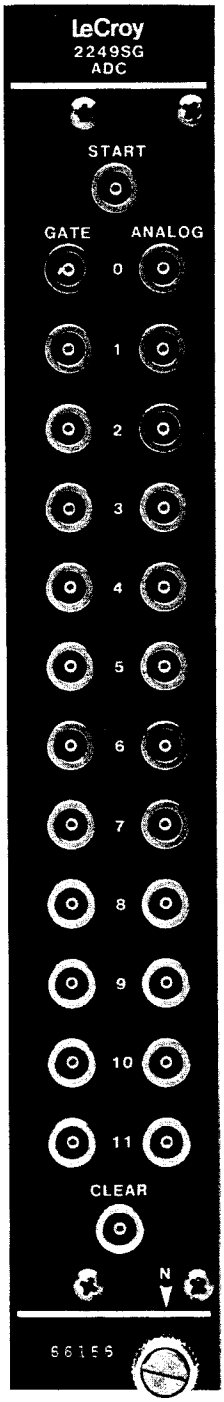
TYPICAL 2249A INTEGRAL LINEARITY



SPECIFICATIONS SUBJECT TO CHANGE.

TECHNICAL DATA

LeCroy



CAMAC Model 2249SG

12-Channel A-to-D Converter With Separate Gates

The LeCroy Model 2249SG 12-Channel Analog-to-Digital Converter is a separately gated version of the world's most widely used integrating ADC, the Lecroy Model 2249A. It embodies all the operational characteristics which have proved important for general-purpose use in high energy particle physics, including high resolution, high sensitivity, excellent stability, fast digitizing rate, LAM and Q suppression, provision for fast clear, calibrating test mode, and flexible LAM options.

The Model 2249SG contains twelve complete ADC's in a double-width CAMAC module. Each ADC offers a 10-bit conversion to provide a wide 1024-channel dynamic range. The input sensitivity of the Model 2249SG is 0.25 pC/count for a full-scale range of 256 pC. This is compatible with most available signal sources and no additional buffering or reshaping of any kind is required to digitize nanosecond pulses.

The excellent long-term stability, temperature characteristics, and isolation between ADC channels assure accurate and reliable performance under the demanding conditions encountered in actual experiments. Confirmation of operation and calibration is provided by a unique optional test feature which allows all twelve ADC's or an entire system to simultaneously digitize a charge proportional to a dc level provided to a front-panel Lemo connector or patched into P_1, P_2, or P_5 of the Dataway connector.

The Model 2249SG offers excellent event rate capability through the incorporation of a fast clear and a fast digitizing rate. The fast clear input enables each ADC to begin digitizing on the command of a prompt gate and be reset, if necessary, before the end of conversion on the basis of delayed logic or chamber information. This feature eliminates the long input delay cables now required in these situations.

End of conversion of modules which contain data is flagged by generation of a CAMAC LAM. Readout of modules which do not contain information can be eliminated either by use of the LAM signals or through Q suppression.

November 1982

Innovators in Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION • 700 SOUTH MAIN STREET • SPRING VALLEY, N.Y. 10977
TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

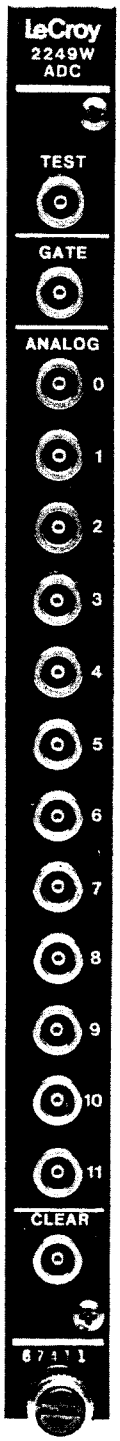
SPECIFICATIONS
MODEL 2249SG
12-CHANNEL ADC WITH SEPARATE GATES

Analog Inputs:	Twelve, Lemo-type connectors; charge-sensitive (current-integrating); direct-coupled, quiescently at approximately +4 mV; 50 Ω impedance; linear range normally −2 mV to −1 V; protected to ± 50 volts against 1 μsec transients.
Full-Scale Range:	256 pC ± 5%.
Full-Scale Uniformity:	± 5%.
Integral Non-linearity:	± 0.25% of reading ± 0.5 pC for > 500 Ω source.
ADC Resolution:	10 bits (0.1%) somewhat degraded to approx. 0.2% by clock unsynchronized with any specific linear gate input.
Long-Term Stability:	Better than 0.25% of reading ±0.5 pC/week (at constant temperature).
Temperature Coefficient:	Typical, 0; max., ±(.03% of reading (in pC) +0.002 t) pC/°C (where t=gate duration in nanoseconds, with 50 Ω reverse termination).
ADC Isolation:	A 5-volt, 20 nsec overload pulse in any one ADC disturbs data in any other ADC by no more than 0.25 pC.
Gate Inputs:	Twelve, one per ADC; Lemo-type connectors; 50 Ω impedance; −1.4 V or greater enables; minimum duration, 10 nsec; maximum recommended duration, 200 nsec (actual limit approximately 2 microseconds with reduced accuracy; partial analog input must occur within 0.5 μsec after opening each gate to preserve accuracy), effective opening and closing times; 2 nsec; internal delay, 2 nsec. All gates should occur within 2 μsec of the "start" pulse (other arrangements require internal resistor change). CAUTION: Subsequent gate signals are NOT INHIBITED after receipt of the first one, so care must be taken to externally prevent the application of more than one gate to each channel until a clear is applied.
Start Input:	A NIM level (> −600 mV) signal of a duration exceeding 10 nsec must be applied to start the internal oscillator. It should be applied simultaneous to the earliest gate pulse or should follow it by no more than 100 nsec.
Fast Clear:	One front-panel input common to all ADC's; Lemo-type connector 50 Ω impedance; −600 mV or greater clears, minimum duration, 50 nsec. (Caution: narrower pulses cause partial clearing.) Requires additional 1.5 μsec settling time after clear.
Test Function:	The standard 2249SG does not respond to F(25) and has no test feature. However, on-line test capability is optional at the expense of the CAMAC "Inhibit". With Q7 (the "inhibit" transistor) removed, the leading edge of a pulse applied to the "start" input will cause a fixed charge to be injected onto the 2249SG analog inputs. Coincident with the "start," the 12 gate pulses must be applied of duration approximately 80 nsec. Proportionality constant is −12.5 pC/volt of dc signal applied to P1, P2 or P5 patch points, for an 80 nsec gate. In this test mode, the gates must precede the "start" by 10 nsec.
Digitizing Time:	Approximately 60 μsec.
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.
Readout Control:	Ready for readout when LAM signal appears. Refer to ESONE Committee Report EUR4100e and EUR4600e or IEEE #583 for additional timing details, voltages, logic levels, impedances, and other standards.
Data:	The proper CAMAC function and address command normally gates the 10 binary bits plus overflow bit of the selected channel onto the R1 to R11 (2^0 to 2^{10}) Dataway bus lines.
CAMAC Commands:	Z or C: ADC's and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. Z also disables LAM. I: Gate input is inhibited during CAMAC "Inhibit" command. (Nonfunctional if unit is modified to provide "Test" feature.) Q: A Q=1 response is generated in recognition of an F(0) or F(2) Read function or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q=0) under any other condition. The Q response for empty modules can be suppressed. (See Q and LAM suppression.) X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated. L: A Look-At-Me signal is generated from end of conversion until a module Clear or Clear LAM. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by Test LAM. Standard option causes LAM to be suppressed for empty modules.
CAMAC Function Codes:	F(0): Read registers; requires N and A, A(0) through A(11) are used for channel addresses. F(2): Read registers and Clear module and LAM; requires N and A; (Clears on A(11) only.) F(8): Test Look-At-Me; requires N and any A from A(0) to A(11) independent of Disable Look-At-Me. Q response is generated if LAM is set. F(9): Clear module and LAM; requires N, S2, and any A from A(0) to A(11). F(10): Clear Look-At-Me; requires N, S2, and A from A(0) to A(11) F(24): Disable Look-At-Me; requires N,S2, and any A from A(0) to A(11). F(26): Enable Look-At-Me; requires N, S2, and any A from A(0) to A(11). Remains enabled until Z or F(24) applied. Caution: The state of the LAM mask will be arbitrary after power turn-on.
Q and LAM Suppression:	Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 100) before data is considered useful. A module in which all channels contain less than set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option.
Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e or IEEE Report #583). RF-shielded CAMAC #2 module.
Current Requirements:	+24 V at 35 mA; −24 V at 15 mA; + 6 V at 850 mA; −6 V at 200 mA.

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



CAMAC Model 2249W
12 Channel Analog-to-Digital Converter

The LeCroy Model 2249W is a 12 channel, 11-bit integrating-type analog-to-digital converter. It features excellent linearity and unprecedented stability, thus allowing operation at wide gates of up to 10 μsec. Thus, the 2249W is compatible with CsI and NaI crystal detectors. Its minimum gate of 30 nsec makes its use with organic scintillators and Cerenkov detectors possible in all but the highest rate conditions.

The 2249W has been optimized for dynamic range and linearity. By AC-coupling the input, 11-bit (1980 counts) operation has been achieved with ± 2 count integral linearity. This excellent linearity is maintained from the smallest signal size to signals as large as −2 V.

The test feature allows all 12 ADC's to simultaneously digitize a charge proportional to a DC level provided to a front-panel connector or patched into the CAMAC Dataway connector. In addition, the pedestals alone can be checked on-line by the same test feature by removing the CAMAC inhibit (I) during the test.

The Model 2249W offers an excellent event rate capability through the incorporation of a 2 μsec fast clear, which permits the ADC's to begin digitizing and then be cleared upon receipt of later trigger information rather than delaying the analog signals with long cables while the trigger decision is being made. In addition, rapid readout is made possible by a convenient Q and LAM suppress feature, side-panel adjustable between 0 and 100 counts. This feature permits an empty 2249W to be overlooked in a CAMAC readout cycle.

Innovators in Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION • 700 SOUTH MAIN STREET • SPRING VALLEY, N.Y. 10977
TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

SPECIFICATIONS
CAMAC Model 2249W
12 CHANNEL ANALOG-TO-DIGITAL CONVERTER

Analog Inputs:	12; Lemo type connectors; charge sensitive (current integrating); AC coupled (2 msec time constant, field changeable); 50 Ω impedance; linear range normally 0 to −2.0 V; protected to ±50 V against 1 μsec transients.
Gain:	−0.25 pC/count ±5%
Full-Scale Range:	Approximately −500 pC (maximum count ≅ 1980)
Integral Non-Linearity:	±0.05% ±(0.5 pC +0.1%)
ADC Resolution:	0.05% (1980 total counts)
Long Term Stability:	Better than 0.25% of reading ±0.5 pC/week (at constant temperature)
ADC Isolation:	A 5 V, 20 nsec overload pulse in any one ADC disturbs data in any other ADC by no more than 0.5 pC (2 counts).
Gate Input:	One gate common to all ADC's; Lemo type connector; 50 Ω impedance; −600 mV or greater enables; minimum duration, 30 nsec; maximum recommended duration up to 10 μsec; partial analog input must occur within 0.5 μsec after opening gate to preserve accuracy; effective opening and closing times, 5 nsec; internal delay, 7 nsec.
Fast Clear:	One front panel input common to all ADC's Lemo type connector; 50 Ω impedance; −600 mV or greater clears, minimum duration, 50 nsec. Requires additional 2.0 μ sec settling time.
Pedestal:	Adjustable over approximately 100 counts via side-panel accessed trimmer capacitor. Somewhat higher for wide gate.
Test Function:	With CAMAC I present, the positive DC level applied to front panel "Test" input (internal high impedance connection to +12 V) or optional rear connector P1, P2, or P5 patch points will inject charge with a proportionality constant of −15 pC/V into all inputs at F(25)•S2 time. (With CAMAC I not present, F(25)•S2 will generate the gate only, providing a measure of the pedestal.)
Digitizing Time:	106 μsec
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.
Readout Control:	Ready for readout when LAM signal appears. Refer to ESONE Committee Report EUR4100e and EUR4600e for additional timing details, voltages, logic levels, impedances, and other standards.
Data:	The proper CAMAC function and address command normally gates the 11 binary bits of the selected channel onto the the R1 to R11 (2^0 to 2^{10}) Dataway bus lines.
CAMAC Commands:	Z or C: ADC's and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. Z also disables LAM. I: Gate input is inhibited during CAMAC "Inhibit" command. (Test function is enabled.) Q: A Q = 1 response is generated in recognition of an F(0) or F(2) Read function or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q = 0) under any other condition. The Q response for empty modules can be suppressed (see Q and LAM suppression). X: An X = 1 (Command Accepted) response is generated when a valid F, N, and A command is generated. L: A Look-At-Me signal is generated from end of conversion until a module Clear or Clear LAM. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by test LAM. Standard option causes LAM to be suppressed for empty modules.
CAMAC Function Codes:	F(0): Read registers; requires N and A; A(0) through A(11) are used for channel address. F(2): Read registers and Clear module and LAM; requires N and A: (clears on A(11) only). F(8): Test Look-At-Me; requires N and any A from A(0) to A(11) independent of Disable Look-At-Me. Q response is generated if LAM is set. F(9): Clear module and LAM: requires N, S2, and any A from A(0) to A(11). F(10): Clear Look-At-Me; requires N, S2 and any A from A(0) to A(11). F(24): Disable Look-At-Me; requires N, S2, and any A from A(0) to A(11). F(25): Test module; requires N, S2 and any A from A(0) to A(11). F(26): Enable Look-At-Me; requires N, S2 and any A from A(0) to A(11). Remains enabled until Z or F(24) applied. Caution: the state of the LAM mask will be arbitrary after power turn-on.
Q and LAM Suppression:	Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 100) before data is considered useful. A module in which all channels contain less than set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accept response is still generated. The LAM suppress portion can be disabled with a solder jumper option.
Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e). RF shielded CAMAC #1 module.
Current Requirements:	143 mA at +24 V; 75 mA at −24 V; 725 mA at +6 V; 155 mA at −6 V

SPECIFICATIONS SUBJECT TO CHANGE

SECTION 2

OPERATING INFORMATION

2.1 General

The LeCroy Model 2249 Series 12-Channel ADC contains 12 complete analog-to-digital converters in a CAMAC module. The 2249A and SG offer 10 bits, and the W version offers 11 bits. The analog-to-digital conversion is accomplished by the Wilkinson-rundown method, which ultimately yields a digital output (in TTL negative logic binary format) which is proportional to the integral of the charge in the input pulse. By the Wilkinson technique, the input charge is delivered to an integrating capacitor from a linear gate, and then discharged at A constant rate. During the time this rundown is taking place, pulses from an oscillator are gated into a scaler resulting in the final count proportional to the charge originally stored in the capacitor.

2.2 Analog Inputs

The 12 analog inputs of the 2249 Series are of 50 Ω impedance and accept negative-going pulses only during an externally applied gate. To assure performance within the linear range, input signals should not exceed -1 volt for the 2249A and SG, or -2V for the W version. The actual amount of input charge that yields a full scale digital output (1024 counts) is 256 picocoulombs (or 12.8 volt-nsec) for the 2249A and SG; 512 pC (25.6 volt-nsec) for the W version. The full scales of the 12 channels of each 2249 are set up to match within ±5% of each other. Quiescent DC level of the analog inputs of the 2249A and SG are set at approximately +4 mV to assure that it does not go negative should any drift occur. The 2249W is AC coupled and does not require this critical biasing.

2.3 Gate

The built-in linear gate is common to all 12 analog inputs of the A and W, necessitating that analog-to-digital conversion for all channels be done in parallel. The 50 Ω impedance gate input of the 2249A and 2249W accepts pulses $\geq$ -600 mV in amplitude (the 2249SG requires twice this amplitude for the gate input as explained below). The gate duration may be between 10 nsec and 200 nsec for the 2249A and 2249SG (see next paragraph). The 2249 W may be used with gate widths between 30 nsec and 10 μsec. Because of the finite risetime and falltime of the internal gate pulse, the effective gating interval is not adequately defined to allow input gate pulses shorter than 10 nsec. The actual gate opening and closing times are approximately 4 nsec, and therefore the gate should precede the analog inputs by at least 4 nsec (A and SG versions) or 7 nsec (W version). Except when photomultiplier noise is a prime consideration, it is good practice to apply a gate pulse which is wider than the expected duration of the longest analog input. IMPORTANT NOTE - The duration of the effective gate will exceed that of the gate pulse by 4 nsec for the A and SG versions and 5 nsec for the W version. The 2249SG gate inputs require -1.4 V to be enabled. Deviations from this amplitude will result in pedestal variations as the charge injection is controlled by the gate pulse. The gate inputs are terminated in 50 Ω allowing one half of the 32 mA current source

output of a NIM module (such as the LeCroy Models 429A or 821) to be employed. The second half of the bridged pair should not be terminated in 50 Ω.

For the 2249A and SG, gate widths exceeding 200 nsec create excessive residual pedestal (1 + 0.03 t/pC, where t = gate duration in nsec) and reduce the overall accuracy of the ADC by magnifying the effects of the instability manifest in the temperature coefficient, which is directly dependent upon the gate width. That maximum is ± (.03% of the reading in pC + .002 t)pC/°C). In addition, longer gates will imply an increased susceptability to any DC offset of the analog input. The actual limit of the gate duration is 2 μsec provided the resultant decrease in accuracy can be tolerated. With a gate duration of >200 nsec, it is recommended that the inputs be AC-coupled if possible.

The excellent stability and linearity of the Model 2249W allows it to be used with gate widths up to 10 μsec. In order to maintain this linearity with wide gates, however, it is necessary for the input pulse to occur within 500 nsec of the gate opening. During this 500 nsec period, a fixed amount of charge is automatically injected onto the integrating capacitor to assure linear operation even for very small input charges which would otherwise deviate from the linearity maintained by the circuit for larger input charges. This injection lasts approximately 500 nsec, but the appearance of charge from the analog input will cause it to be extended. Without input charge appearing, the q inject will cease after 500 nsec (i.e., charge added will settle out), and subsequent input charge would be subject to a conversion graph which is non-linear at the low end (i.e., for small input charges).

Similarly, if it is necessary to use wide gates (>200 nsec) and the 2249W is not available, the 2249A may be used with reduced accuracy. In this case, the analog input should also occur within 500 nsec after the gate opening.

The 2249 Series gate is inhibited from shortly (100 nsec) after the trailing edge of the gate until any CAMAC clear (C, Z, F(9) or F(2)·A(11)) or a front panel clear is applied. This effectively locks out spurious analog signals and noise from the ADC while the desired signal is being processed. The ADC's internal oscillator is synchronized with the leading edge of the gate pulse (although it occurs somewhat later), eliminating inaccuracies which could be caused by the utilization of free-running oscillators.

2.4 Start Input (2249SG Only)

Because the gate inputs of the 2249SG are considered asynchronous, a separate signal is required to start the internal oscillator. This pulse should be a NIM level applied either simultaneously with the earliest gate pulse or should follow it by ≤ 100 nsec. The pedestal of a given channel will decrease by 1 count per 50 nsec start delay, with respect to the Gate time.

2.5 Fast Clear

A front panel fast clear input accepting NIM-level signals (≥ 50 nsec in width) forces all 12 channels to cease their conversions, be cleared and ready to accept another gate pulse after 1.5 to 2.0 μsec (see Technical Date sheets at the beginning of this manual). An internal monstable makes this

wait period mandatory. The fast clear feature allows ADC conversion to begin on a fast trigger and be completed only if the event satisfies a complete trigger requirement.

2.6 Test Feature

A built-in test feature checks all channels simultaneously with an F(25) command. If the CAMAC Inhibit (I) is present and a positive DC level is applied either to a front panel "Test" input (with internal high $Z \geq 10$ KΩ connection to +12 volts) or optionally to rear connector patch points P1, P2, or P5, then F(25)•S2 will inject charge with a proportionality constant of approximately -12.5 pC/volt into all inputs (20 pC for the W version). A 20 Volt test input will correspond to nearly full scale output. The internal gate generated by F(25)•S2 is approximately 80 nsec. If the user desires a measure of residual pedestal only, the CAMAC "I" should be removed; F(25)•S2 will then generate the 80 nsec gate only with no charge being injected into the analog inputs. This test feature permits the pedestal itself to be periodically checked for drifts. If two measurements are made, one with charge input and one without (i.e., with and without "I"), the total conversion characteristics could be checked. In this case, the "no charge" result gives the intercept and the "with charge" counts minus the "without charge" counts divided by the charge applied, gives the slope of the conversion plot. See Figure 2.1.

The test feature may be connected to the rear of the 2249 as mentioned previously. The rear of the 2249 printed circuit board contains 3 drilled holes labeled P1, P2, and P5. Soldering a feedthrough at any one of these holes electrically connects the front panel "Test" input to the CAMAC connector pins P1, P2, or P5. In this way, many units can be grouped for simultaneous calibration.

It should be noted that the standard 2249SG does not respond to F(25) and has no "Test" feature. It is possible, however, to do on-line testing of the 2249SG if necessary. The price of this feature is the elimination of the inhibit feature. With the standard 2249A, the CAMAC "Inhibit" enabled the test circuit while disabling the gate circuit. Since the 2249SG has no internally generated "Test" function, the "Start" circuit must be used. To permanently enable this "Start" circuit to permit a test function to be performed, Q7, or the inhibit transistor, must be removed.

With Q7 removed, the leading edge of a pulse applied to the "Start" input will cause a fixed charge to be injected into the 2249SG analog inputs. Coincident with the "Start", the 12 gate pulses must be applied, which should have a duration between 80 nsec and 100 nsec. An exact 80 nsec gate will yield a proportionality constant of -12.5 pC/volt of DC signal applied to whichever rear patch point (P1, P2, or P5) you choose to use for the test input. For shorter gate widths, a smaller net amount of charge is injected into each input, i.e., on the order of 90% $\pm$ 1% for a 40 nsec gate.

If a test function is to be used, care must be taken to be sure the "gates" precede the "Start" by 10 nsec.

CAUTION: Since the "Test" is not a designated feature of the 2249SG, its utilization is not factory tested.

2.7 Linearity

The integral linearity of the 2249 Series is typically < ± 2 counts (see specifications in Technical Data Sheet, Section 1). This is defined by LeCroy as the maximum deviation from the best straight line fit to measured points. Every ADC is computer tested before being shipped to make certain it meets linearity and functional operation specifications. Each channel is tested for linearity at 21 points across its range by a 16 bit digital to charge converter.

2.8 Pedestal

The residual pedestal is the number of counts obtained when a gate pulse is applied with a no analog input (i.e., input merely terminated in 50 Ω). Pedestal is a result of several factors, the largest of which is the charge injection (also contributing to the A and SG versions is a factory-set positive DC offset) the purpose of which is to assure proper operation of the front end in case the quiescent DC level of the input should drift. It is this DC offset contribution which largely comprises the gate-dependent portion of the residual pedestal specification. The fixed amount of pedestal indicated on the technical data sheet results largely from the charge injection.

Due to DC coupling of the A and SG inputs, the gate-dependent portion of the pedestal has a temperature coefficient associated with it. This effect is magnified by a factor of 2 if the input is DC shorted to ground as it would be when driven from a pulse transformer, for example, used to cater photomultiplier dynode signals to the negative input requirements of the 2249A. For short gate widths, the resultant potential temperature drift is small. However, it is nevertheless recommended that AC-coupling be used wherever rate conditions can permit it. This will nearly eliminate all but the fixed pedestal and its associated temperature coefficient.

The pedestal of the 2249A is factory adjusted to approximately 8 counts for a gate duration of 50 nsec and to 50 counts for the SG version. The pedestal of the 2249W is factory adjusted to approximately 16 counts for a gate duration of 400 nsec. The adjustment is made with 50 Ω termination of each analog input. The pedestal of each channel of the 2249A is separately screwdriver adjustable through the side panel. Each adjustment screw is accessed through a hole adjacent to the input for the channel. (NOTE: When making adjustments, use a non-conducting screwdriver.)

2.9 Conversion Time

Since the full scales of the 12 channels of each 2249 may differ from each other by up to ± 5%, the time for each channel to achieve a full scale conversion may also differ from that of the other channels. Total conversion time is roughly 50 µsec for the A and SG versions and 100 µsec for the W version. Manufacturing variances in clock frequency, ramp currents, and the necessity to allow for overflow as well as a wait interval incorporated in the design, require that a 20% margin in conversion time be allowed for. As a result, the 2249A clock is internally held on for a maximum time of 60 µsec, the SG for 55 µsec, and the W for 100 µsec (for