Chapter 4

P0/J0 Connector Area and VME64x Backplane End Dimensions

4.1 Introduction

At times manufacturers and users of VME64x boards have a need for additional and sometimes specialized I/O through the backplane. This chapter specifies the requirements and provides observations for implementation of user defined I/O between the P1/J1 and P2/J2 connectors.

This area is commonly called the P0/J0 connector area, even though four connectors are involved: a connector on the front VME64x board (P0), a connector on the front of the backplane (J0), a connector shroud on the rear of the backplane (RJ0) and a connector on the rear board (RP0) or the end of cable which plugs into the rear connector. This is sometimes written as: P0/J0/RJ0/RP0, where the "R" means rear. (The rear connector shroud goes over the long tail pins and provides the necessary alignment and other mechanical support for normal connector mating.)

See Chapter 9 for the definition of rear I/O transition boards and for mechanical alignment with the backplane. See Figure 9-1 for a pictorial of the connector placements on VME64x boards, VME64x backplanes and rear I/O transition boards.

Due to usage of the J0, 2 mm connector, VME64x backplane's left and right end mechanical dimensions are shifted left, to accommodate the connector's added width and position. Section 4.2.7 defines VME64x backplane's left and right end dimension.

4.2 Requirements

Permission 4.1:

Additional user defined I/O connector space may be obtained if the mechanical member between J1 and J2 connector pairs on VME backplanes, shown in Figure 7-18 of the VME64 Standard, is removed.

Rule 4.1:

Whenever a structural member is not used between the J1 and J2 connectors on VME64x backplanes, the VME64x backplane shall maintain sufficient rigidity to meet the mechanical requirements specified in IEEE 1101.1.

Observation 4.1:

VME64x boards using I/O connectors between P1 and P2 could conflict with VME/VME64 backplanes that have a structural member between J1 and J2 connectors.

4.2.1 Connector Selection

Rule 4.2:

For generic use the 19 position, Type B, 2 mm hard metric, IEC 61076-4-101 connector family shall be used. The connectors shall be rated Performance Level 2 or better with a minimum of 250 insertion withdrawal cycles.

Rule 4.3:

For generic uses, the 19 position, Type B, 2 mm hard metric IEC 61076-4-101 free board connector shall be used on VME64x boards.

Rule 4.4:

For generic uses, the 19 position, Type B, 2 mm hard metric IEC 61076-4-101 fixed board connector shall be used on the VME64x backplanes. On the front side, rows z

and f shall be length 3 (11.2 mm) and rows a through e shall be length 1 (8.2 mm). On the rear side, the pin tail lengths shall be 16 mm when straight through I/O is used, or less than 5.0 mm when a sub-bus is used.

Rule 4.5:

When straight through I/O is used, a shroud over the rear long tail pins shall be used that meets the mechanical dimensions defined in IEEE P1101.11.

Rule 4.6:

Where the 2 mm hard metric IEC 61076-4-101 connector is used, the z and f row pins on the backplane's fixed board connector shall be connected to the backplane's ground plane as defined in Table 4-1, P0/J0 Connector Pin Labeling.

Rule 4.7:

The z row shield on the free board P0 and RP0 connectors shall only be used if it does not protrude through the board's interboard separation plane, as defined in IEEE 1101.1.

Observation 4.2:

Some of the 2 mm hard metric connector's z shields protrude into the interboard separation plane, and therefore can not be used.

Observation 4.3:

The two outer rows of contacts are connected to ground on the backplane. When only the f row shield is used on the free board connector, 19 ground contacts are supplied to the board. The use of both the f and z row shields provide a total of 38 ground contacts.

4.2.2 Custom Connectors

Permission 4.2:

Custom I/O connectors such as coaxial cable or fiber may also be used on VME64x boards and VME64x backplanes which require specialized custom I/O in the P0/J0 connector area.

Observation 4.4:

VME64x backplanes with custom I/O connectors will not be compatible with VME64x boards containing a P0 connector per Rule 4.2.

Recommendation 4.1:

The keying scheme defined in this standard should be used for boards and backplane slots that have custom I/O connectors.

Recommendation 4.2:

For applications that are 1101.2 based, the VITA 1.6-199x Keying for Conduction Cooled VME draft standard should be used.

Rule 4.8:

Any custom connector installed on the backplane in the J0 connector area shall allow the front board's rear edge to be installed (come to rest) within 12.5mm of the backplane surface.

Observation 4.5:

A connector with a height of greater than 12.5mm will protrude over the rear edge of a VME64x board when fully inserted into a slot. This would prevent generic boards, that do not have a mating P0 connector, from being inserted into that slot.

4.2.3 P0/J0 Pin Definitions

Rule 4.9:

The row and column labeling of the contacts in the P0/J0/RJ0/RP0 connector shall be as shown in Table 4-1, P0/J0/RJ0/RP0 Connector Contact Labeling.

Table 4-1 P0/J0/RJ0/RP0 Connector Contact Labeling

Pos.	Row f	Row e	Row d	Row c	Rows b	Row a	Row z
1	GND	UD	UD	UD	UD	UD	GND
2	GND	UD	UD	UD	UD	UD	GND
3	GND	UD	UD	UD	UD	UD	GND
4	GND	UD	UD	UD	UD	UD	GND
5	GND	UD	UD	UD	UD	UD	GND
6	GND	UD	UD	UD	UD	UD	GND
7	GND	UD	UD	UD	UD	UD	GND
8	GND	UD	UD	UD	UD	UD	GND
9	GND	UD	UD	UD	UD	UD	GND
10	GND	UD	UD	UD	UD	UD	GND
11	GND	UD	UD	UD	UD	UD	GND
12	GND	UD	UD	UD	UD	UD	GND
13	GND	UD	UD	UD	UD	UD	GND
14	GND	UD	UD	UD	UD	UD	GND
15	GND	UD	UD	UD	UD	UD	GND
16	GND	UD	UD	UD	UD	UD	GND
17	GND	UD	UD	UD	UD	UD	GND
18	GND	UD	UD	UD	UD	UD	GND
19	GND	UD	UD	UD	UD	UD	GND

Observation 4.6:

The J0/RJ0 connectors have seven physical rows of contacts, with the z and f contact rows connected to the backplane's ground plane. On the VME64x board, there is no z row of contact holes Depending on the connector design, the P0 and RP0 connector ground contacts in the z and f row of the connector (which is on the connector shroud) will alternately connect to the board's f row of ground contacts.

Observation 4.7:

Connector layout and position numbering method is the same as the P1/J1 and P2/J2 connectors. Position 1 is near P1/J1's position 32 and position 19 is near P2/J2's position 1.

4.2.4 P0/J0 Connector Mounting

Rule 4.10:

Mounting of the 19 position, 5+1 row, Type B, 2 mm hard metric IEC 61076-4-101 free board connector on VME64x boards shall be as shown in Figure 4-1, when implemented

Rule 4.11:

Mounting of the 19 position, 5+2 row, Type B, 2 mm hard metric IEC 61076-4-101 fixed board connector on VME64x backplanes shall be as shown in Figure 4-2, when implemented.

4.2.5 Pin Current Ratings

Rule 4.12:

The maximum current load per contact shall be in compliance to the IEC 61076-4-101.

Observation 4.8:

When the ANSI/VITA 1.1, VME64x standard was approved, the maximum current load per contact was defined to be 2.0 amp at 70° C when an alternate chess pattern of contacts are used for power. When adjacent contacts are grouped together for power, the maximum current per contact is 1.0 amp at 70° C. The current rating of the shield contacts in rows z & f is 1.5 amp at the same temperature. For power ratings at other temperatures, see IEC 61076-4-101.

Rule 4.13:

The shield contacts are connected to logic ground on the backplane and boards. It is not connected to frame ground. Although the shield contacts will provide a ground return path the current carrying capacity of the pins shall not be used in calculating the overall ground current carrying capacity.

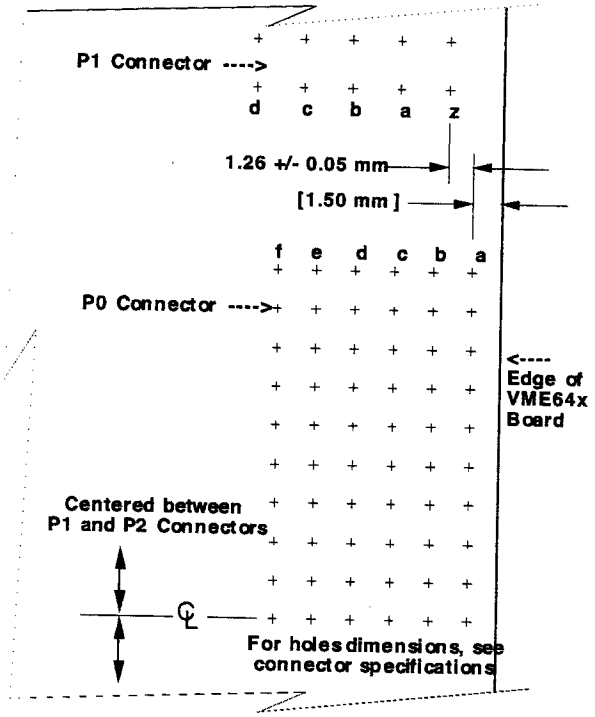

Figure 4-1 P0 Connector Layout Position on VME64x Boards

(component side - top view)

4.2.6 Backplane P0/J0 Keying

In some applications a slot board to backplane keying is required. In particular, IEEE 1101.2 type applications do not use the front panel, but do require slot keying.

Recommendation 4.3:

For applications that need a slot board to backplane keying capability, the keys defined in VITA 1.6-199x Keying for Conduction Cooled VME should be used.

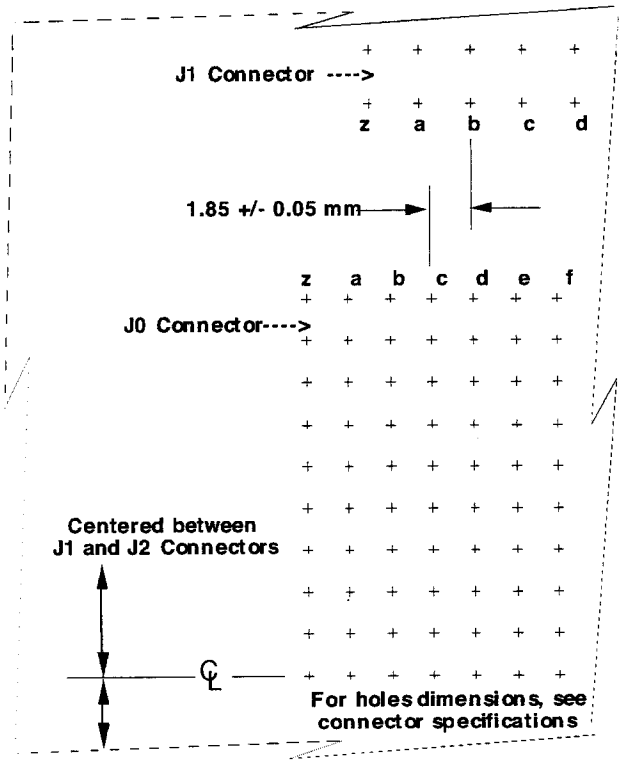

Figure 4-2 J0 Connector Layout Position on VME64x Backplanes

(front view)

4.2.7 VME64x Backplane End Dimensions

Mounting of the J0 2 mm connector on VME64x backplanes causes the backplane to be shifted to the left on both the left and right ends, over VME/VME64 backplanes. Only the two end dimensions are affected. All the other backplane dimensions remain the same as defined in the VME64 Standard.

When two VME64x backplanes of less than 21 slots are mounted next to one another in the same subrack, the gap between the two backplanes is designed to be 1 mm. In the VME64 Standard, this dimension is defined as 1.44 mm. Depending on the specific application needs, backplanes can be made wider. The incremental width needs to be consistent such that when backplanes are mounted next to one another or mounted next to other hardware, such as disk drive or power supplies, the gap always remains the same, regardless of the backplane width and number of slots used.

Rule 4.14:

The left and right end dimensions of minimum width VME64x backplanes shall be as shown in Figure 4-3.

Rule 4.15:

If VME64x backplanes need to be made wider, the incremental end dimensions for both left and right ends shall be in 5.08 mm (1 HP) increments.

Permission 4.3:

For subrack airflow management purposes, the right end of 21 slot sized VME64x backplanes may extend over the last interboard separation plane by 1.54 +0.00 -0.15 mm.

Rule 4.16:

Half shears shall not exceed 1.00 mm in height when used in VME64x applications.

Observation 4.9:

Note that half shears are commonly used on side (end) plates of subracks to prevent rotation and ensure accurate alignment of subrack horizontal members.

Rule 4.17:

Some side (end) plates that utilize half shears for positioning of horizontal members, shall not place half shears in the area of the backplane ends, as shown in Figure 4-3.

Observation 4.10:

All the other backplane dimensions and tolerances remain the same as defined in the VME64 Standard.

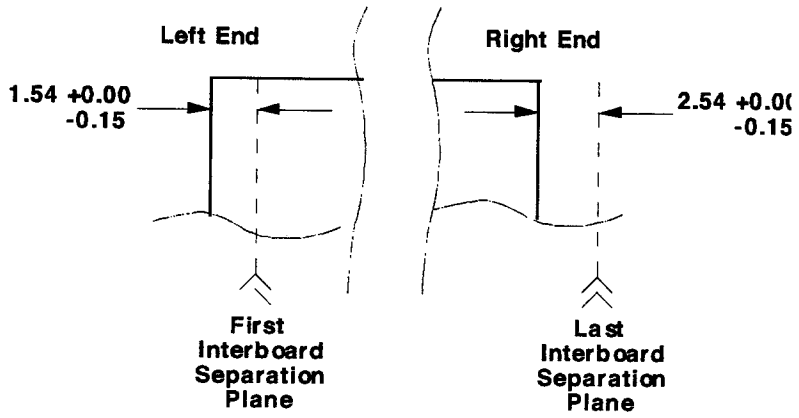

Figure 4-3 VME64x Backplane Left and Right End Dimensions

(front view)

Observation 4.11:

The left end of VME64x backplanes extends over the interboard separation plane by 1.54 mm whereas the right edge of VME/VME64 backplanes are 0.72 mm from the interboard separation plane. Attempting to mount a VME64x backplane to the right of VME/VME64 backplane, while trying to avoid wasting slot space, will result in overlapping of the two backplanes. On the other hand, the right edge of a VME64x backplane can be mounted next to the left edge of a VME/VME64 backplane without mechanical interference in consecutive occupied positions.

Chapter 5

EMC Front Panels and Subracks

5.1 Introduction

This chapter specifies the optional usage of EMC front panels on VME64x boards. In some applications, there is a need to restrict the amount of EMI and RFI being radiated from the front of VME64x subracks, without the aid of a special cover. The EMC front panels and subracks specified in IEEE 1101.10, will provide this capability.

In some applications there is a need for attachment of identification and/or bar code labels on the front panel. This chapter defines three recommended areas that VME64x board suppliers might want to leave open for attachment of special labels.

Note that for VME64x boards and subracks being built according to IEEE 1101.2, IEEE Standard for Mechanical Core Specifications for Conduction-Cooled Eurocards, the EMC design defined in this chapter is not applicable.

5.2 Requirements

5.2.1 EMC Front Panels and Subracks

Rule 5.1:
VME64x boards that require the use of an EMC front panel shall use the EMC front panel as specified in IEEE 1101.10.

Rule 5.2:
If filler panels are used in conjunction with VME64x boards that have EMC front panels, the filler panels shall provide EMC protection. Filler panels shall comply with the filler panels as specified in IEEE 1101.10.

Rule 5.3:
VME64x subracks that are to be used in conjunction with VME64x EMC front panels shall meet the subrack specification given in IEEE 1101.10.

Rule 5.4:
The EMC front panels shall not be electrically connected to the board's logic ground plane nor the ESD strips (if implemented).

Rule 5.5:
Whenever EMC front panels are implemented, the associated alignment pin on the front panel and alignment hole in the subrack defined in IEEE 1101.10 shall also be used to keep boards properly positioned in the subrack.

5.2.2 Solder Side Covers

Recommendation 5.1:
Covers defined in IEEE 1101.10 should be used on the solder side of VME64x board's PCB to prevent scraping of components and the stubs of through hole components by the adjacent left slot's EMC contacts. (This recommendation does not apply to IEEE 1101.2 based boards.)

5.2.3 Front Panel Label Areas

Recommendation 5.2:
An area of 15 mm high by 20 mm wide should be left open at the bottom of VME64x board's front panels for attachment of identification and/or bar code labels. See Figure 5-1, Front Panel Label Areas.

Recommendation 5.3:

Or, an area of 70 mm high by 10 mm wide should be left open on the bottom left side of VME64x board's front panels for attachment of identification and/or bar code labels. See Figure 5-1, Front Panel Label Areas.

Recommendation 5.4:

Or, an injector/extractor handles should be used with a flat surface on the inside of the handle with a dimension of 15 mm wide by 20 mm long for attachment of labels. See Figure 5-2, Injector/Extractor Handle Label Area.

Recommendation 5.5:

Labels attached on the inside of the injector/extractor handles should have a wear resistance coating since this surface is used to apply pressure while removing VME64x boards from a backplane.

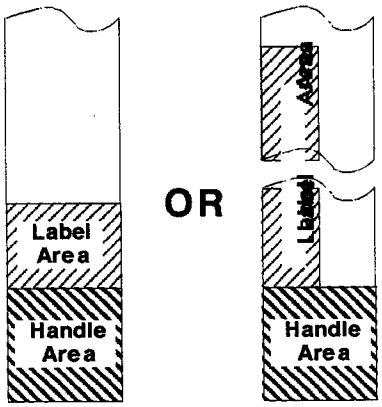

Figure 5-1 Front Panel Label Areas

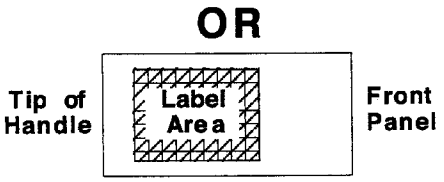

Figure 5-2 Injector/Extractor Handle Label Area
(top view of lower handle)

Chapter 6

Injector/Extractor Handles

6.1 Introduction

In some applications, there might be a need for mechanical assistance during the insertion and/or removal (extraction) of VME64x boards into and out of VME64x subracks. An optional Injector/Extractor Handle and associated subrack defined in IEEE 1101.10 is ideal for this purpose.

The use of screws to secure VME64x boards to VME64x subrack is not allowed in some applications. The screw heads can get damaged, plus the usage of a tool is required to remove and replace VME64x boards from a subrack. A self locking feature in the handle replaces the need for front panel screws and will prevent VME64x boards from falling out under harsh conditions, such as earthquakes, transportation and other high vibration applications.

Note that for VME64x boards and subracks being built according to IEEE 1101.2, the injector/extractor handle design defined in this chapter is not applicable.

6.2 Requirements

6.2.1 Handles

Rule 6.1:
If an Injector/Extractor Handle is used on VME64x boards, it shall be in compliance with the handle defined in IEEE 1101.10.

Recommendation 6.1:
Injector/Extractor Handle that have a self locking feature should be used, which would eliminate the optional use of front panel screws.

Observation 6.1:
The Injector/Extractor Handle is backwards compatible to original VME handles, which allows boards using this handle to be plugged into original VME subracks.

Observation 6.2:
For IEEE 1101.2 based applications, the handles defined in this chapter are not applicable. The handles defined in IEEE 1101.2 are used.

Suggestion 6.1:
In high vibration applications (e.g. military), it may be necessary to use the front panel screws for securing the boards into the subrack.

6.2.2 Subracks

A special Injector/Extractor Handle engagement comb is required on the front of VME64x subracks that will support the use of the referenced Injector/Extractor Handle.

Rule 6.2:
If a VME64x subrack is used that supports the use of the Injector/Extractor Handle, it shall be in compliance with the one defined in IEEE 1101.10.

Observation 6.2:
VME and VME64 boards are forward compatible and can be plugged in to the VME64x subracks.

Chapter 7

Keying and Alignment Pin

7.1 Introduction

In many applications with I/O through the backplane's user defined pins, specific boards are assigned to specific slots. Plugging the wrong board into a pre-defined slot might cause the system to operate improperly. Also, in some applications which assign some of the I/O pins to special power voltages, plugging a board into the wrong slot could have disastrous results. This might include the destruction of the board being plugged in as well as other boards in the same subrack. This becomes even more critical in hot swap applications. Therefore there is the need for keying, where only keyed boards can be plugged into keyed subrack slots.

An optional keying mechanism for VME64x subracks and boards is defined in IEEE 1101.10. This keying mechanism provides for three keying holes on the top and three keying holes on the bottom of each board and each subrack slot. Each keying hole can be keyed with a "No Key" or a keying peg in one of four positions. This effectively provides 5 key combinations per keying hole. With three keying holes on the top and three on the bottom, this keying scheme provides a total of 5 x 5 x 5 x 5 x 5 x 5 = 15,625 keying combinations.

A "No Key" hole in the subrack allows for a "family" of boards to be plugged into a specific slot. Boards with no keys installed can be plugged into any slot, as well as subrack slots with no keys installed will allow for any board to be plugged into the subrack's slot.

The actual number of "hard" combinations, where all holes are keyed in both the board and subrack slots is 4 x 4 x 4 x 4 x 4 x 4 = 4,096 combinations. In applications where both the top and bottom have identical keys, then 4 x 4 x 4 = 64 keying combinations are possible.

An alignment pin and associated alignment hole is to be used as part of the keying mechanism for better alignment during hot swap, for an ESD path from the front panel and for a solid keying blockage if the wrong board is inserted into a keyed slot.

Note that for VME64x boards and subracks being built according to IEEE 1101.2, IEEE Standard for Mechanical Core Specifications for Conduction-Cooled Eurocards, the keying and alignment design defined in this chapter is not applicable.

7.2 Requirements

Observation 7.1:

The features defined in this chapter are not applicable to IEEE 1101.2 based applications.

7.2.1 Subrack Keying

Rule 7.1:

If keying is provided in VME64x subracks, the keying mechanism defined in IEEE 1101.10 for subracks shall be used.

Observation 7.2:

Subrack keying hole positions and associated keying codes for each keying hole are defined in IEEE 1101.10. For information purposes, Figure 7-1 illustrates this subrack keying scheme.

7.2.2 Board Keying

Rule 7.2:

If keying is provided on VME64x boards, the keying mechanism defined in IEEE 1101.10 for boards shall be used.

Observation 7.3:

Board keying hole positions and associated keying codes for each keying hole are defined in IEEE 1101.10. For information purposes, Figure 7-1 illustrates this board keying scheme.

Observation 7.4:

Note that the board keying hole sequence and associated keying position codes is reversed to the subrack when viewing the front of the keying holes.

7.2.3 Keying Number Identification

Recommendation 7.1:

For consistency within each application and between applications, each subrack's slot key and each board's key should use a 6 digit alpha-numeric code, with a slash "/" between the first three digits and last three digits. This sequence follows the letter position of the keying holes, ABC/DEF. The key codes for each position is numbered "1" through "4" as illustrated in Figure 7-1. When "No Key" is used, the letter "N" should be used to indicate that "No Key" is used in the keying hole.

Observation 7.5:

Boards with a key code of 233/423 can only be plugged into a slot with the same key code of 233/423 when keys are used in all the subrack key hole positions. Boards with a keying code of 24N/11N can be plugged into any subrack slot with key codes of 24x/11x, where x is equal to N, 1, 2, 3 or 4.

7.2.4 User Defined and User Installed

The above keying scheme provides user defined and user installed keying combinations.

Recommendation 7.2:

Manufacturers (suppliers) of subracks and boards with keying capability should produce (ship) subracks and boards without the keys installed.

Recommendation 7.3:

Each application (user) should define the keying combinations as required by the application's specific needs and then install the keys accordingly.

Recommendation 7.4:

End users should purchase the keys required for their specific application.

7.2.5 Multifunction Alignment Pin

Rule 7.3:

The multifunction alignment pin defined in IEEE 1101.10 on the rear side of the front panel and the alignment hole next to the subrack keying block shall be used whenever the front panel and/or subrack keying mechanism is implemented.

Observation 7.6:

The multifunction alignment pin and associated hole in the subrack keying block provides the following benefits:

1) Alignment of boards to the backplane connector for a more uniform connector mating during hot swap,

2) A discharge path for any accumulated ESD energy on the front panel and the human operator,

3) A much tighter and more positive contact of the keying pins if a board is mis-keyed with the subrack's slot during insertion.

4) Proper EMC gasket and front panel alignment when boards are plugged into the subrack.
5) A high current connector contact for Front Panel Safety Ground (see section 8.2.5)

Observation 7.7:
The alignment pin might not interoperate with some original subracks that were not designed in compliance with IEEE 1101.1,

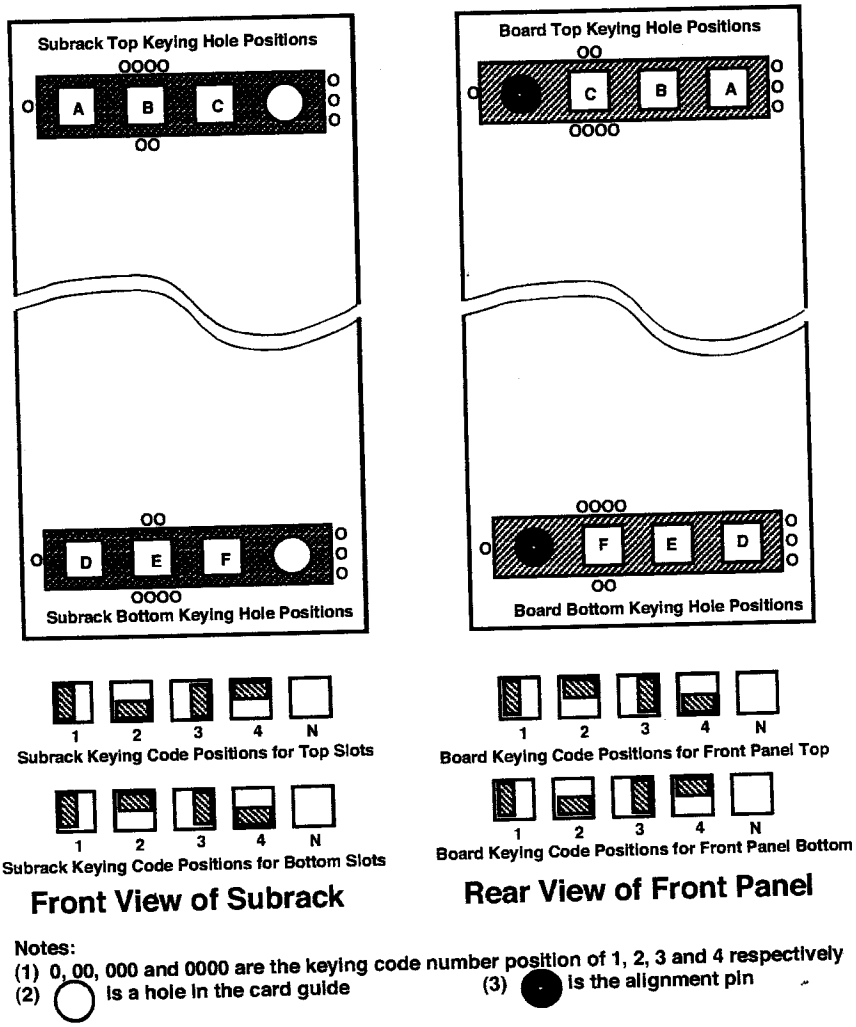

Figure 7-1 Keying Hole Positions and Associated Keying Codes